1997 MTT Presentation

Stabilizing Mosfet Amplifiers

Polyfet Rf Devices
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Stabilizing Mosfet Amplifiers

- Series Gate Resistance
- Shunt Gate Resistance
- Drain Gate Feedback
- Drain Shunt Resistance
- Ferrite Loading (Gate Circuit)
- Ferrite Loading (Drain Circuit)
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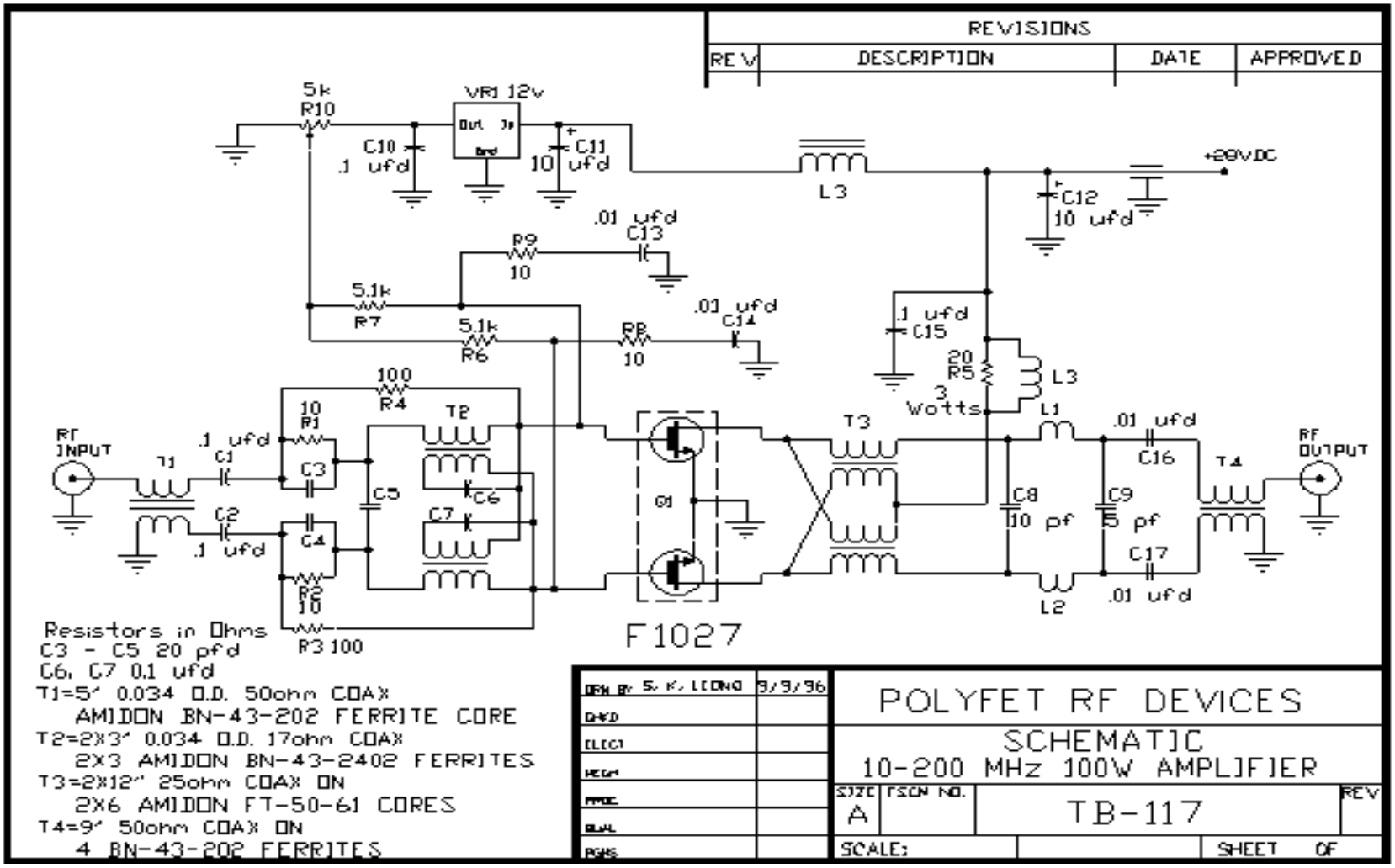
Series Gate Resistance

Series gate resistance increases the loss of any shunt impedance terminating the gate terminal. At frequencies where the gate input impedance is negative, the series resistance prevents oscillation by effectively canceling the negative resistance of the active device. Usually the region of instability occurs at low frequencies so this resistor can be shunted with a capacitor to allow improved high frequency performance. An example of this technique can be found in TB-117 - R1/C3; R2/C4

TB 117

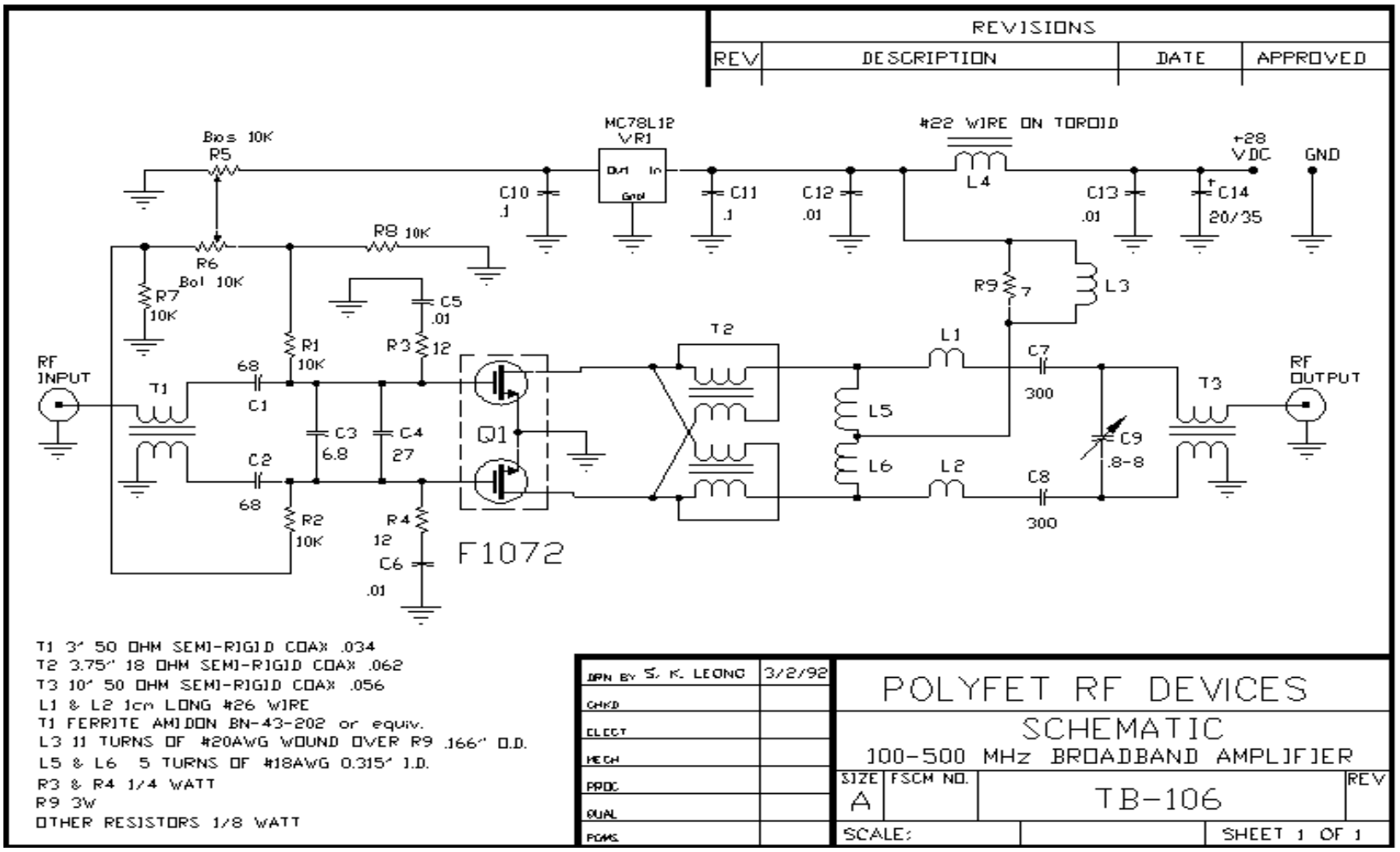


This is an example of a HF to VHF broad band 100 watt power amplifier. Using a 6 + 6 F1B FET, more than 100 watts is available from 10 - 200 MHz. A unique gain sloping is used in the input circuit which maintains a gain flatness to +/- 1 dB across the entire band with - 15 dB input return loss. The output match is accomplished by a 4:1 coaxial transformer followed by a balun.

Shunt Gate Resistance

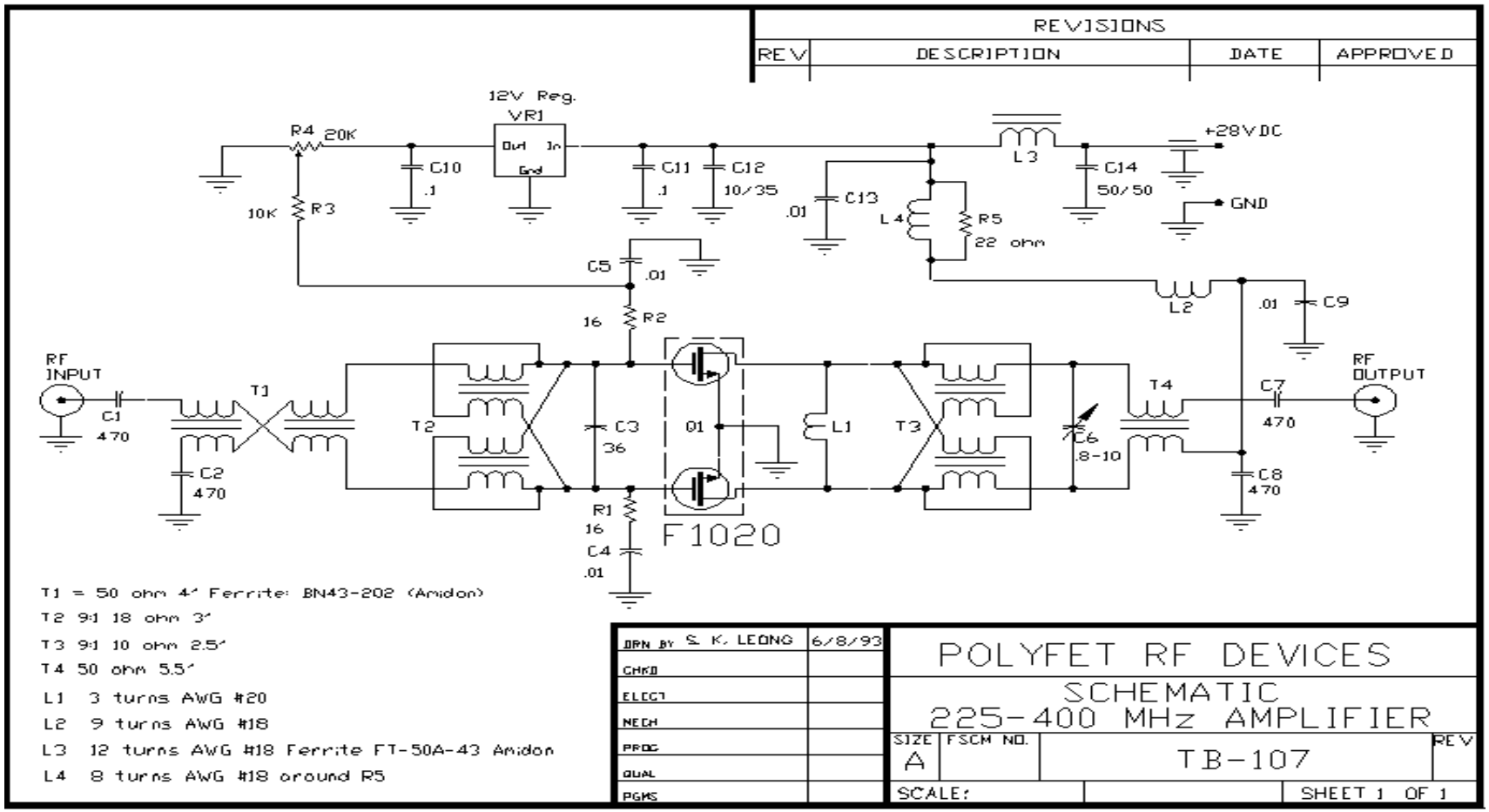
Shunt gate resistance increases the loss of any series impedance terminating the gate terminal. At frequencies where the gate input impedance is negative, the shunt resistance prevents oscillation by effectively canceling the negative resistance of the active device. Usually the region of instability is at low frequencies so an inductor may be placed in series with this shunt resistor to improve high frequency performance. Shunt gate resistance is the most common form of FET stabilization. Some examples of this technique can be found in TB 106 (R4/C6), TB 107 (R1/C4), TB 109(R10/C16) etc.

TB 106



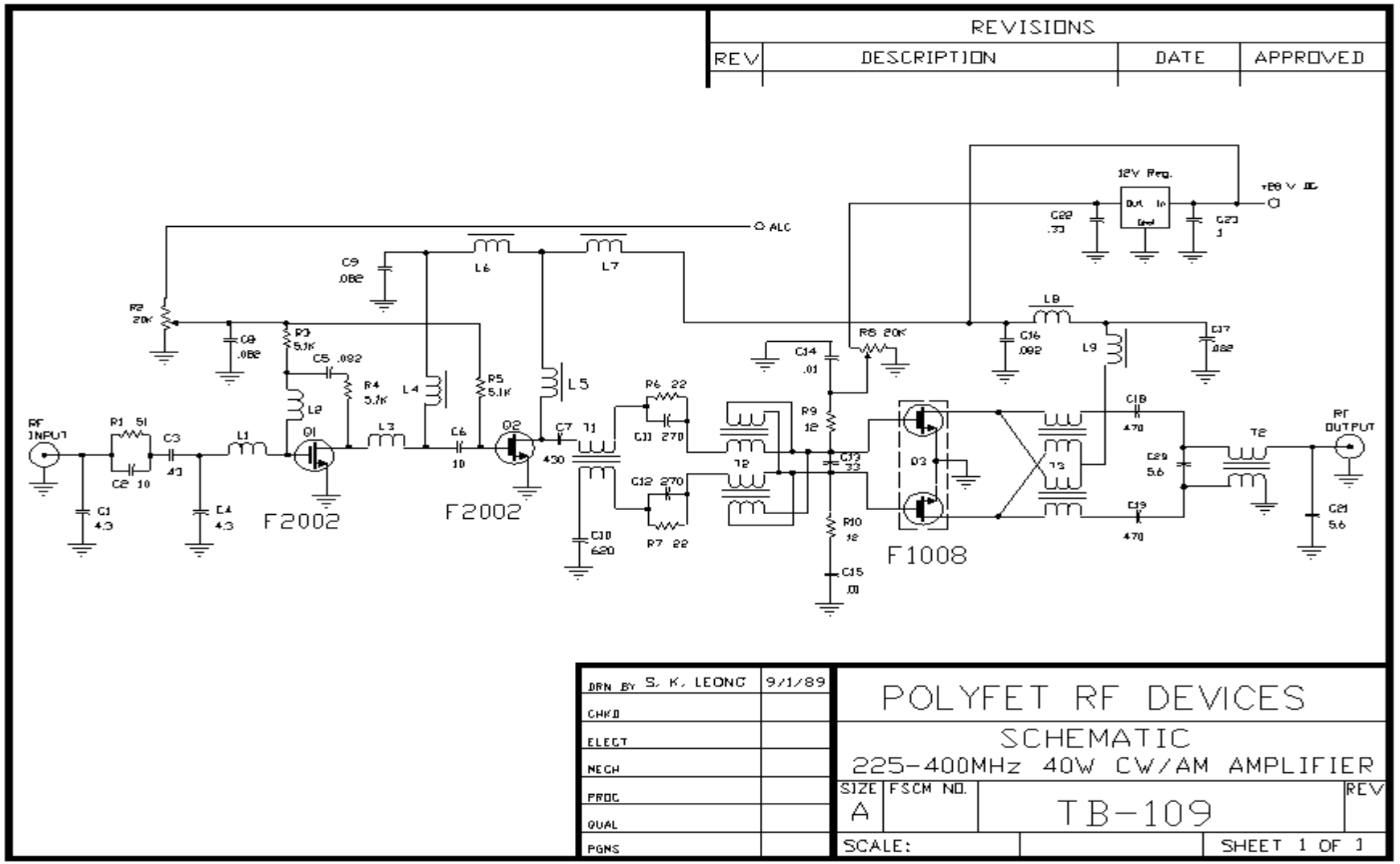
This is a single stage balanced 100 - 500 MHz 80 watts design.. It is intended for use in any application from civilian, military communication bands and ECM and EMI. It utilizes a coaxial balun input transformer and a 9:1 coaxial output transformer, a 3 + 3 F1B device and a coaxial output balun to achieve nearly flat 10 gain at 80 watts output power. The 9:1 output transformer serves dual functions - to match the real and reactive component of the FET.

TB 107



This is a 225 - 400 MHz 130 watt balanced amplifier design. Intended for application in the military communication band which includes SATCOM. The design uses a 5 + 5 F1B device to develop the power level required. Input impedance matching is achieved by utilizing an input balun followed by a 4:1 coaxial step down transformer. Capacitor C3 tunes out the inductive input impedance of the FET. The output match is accomplished by tuning out the capacitive reactance of the FET by L1 and stepping up the impedance with a 4:1 coaxial transformer. A coaxial balun converts the balanced output to single ended.

TB 109

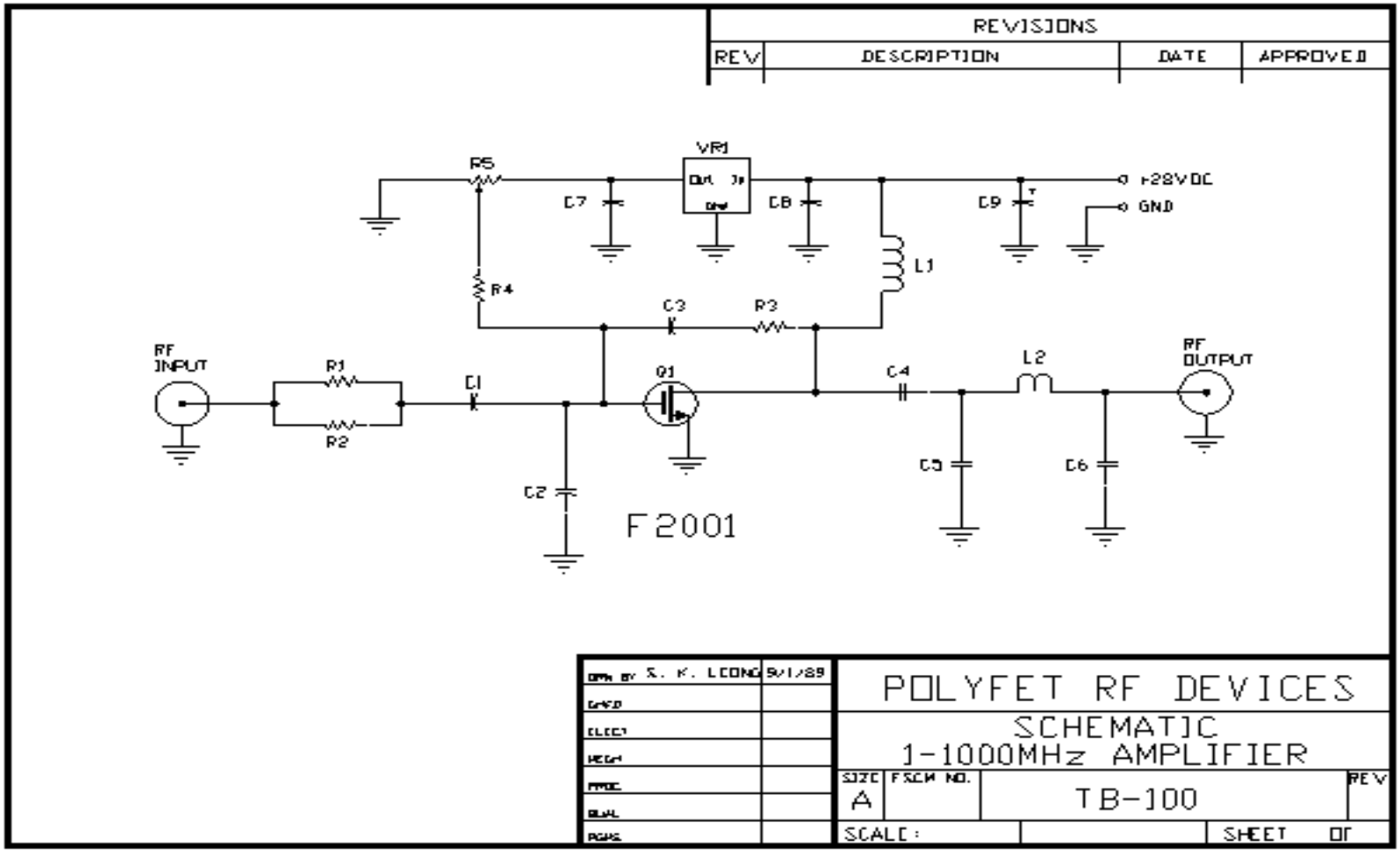


This is a three stage 40 watt PEP military communication band transmitter lineup. The first two stages are operated in class A so they are single ended. The output stage is a balanced design to minimize the second harmonic generation as in TB108. The gain is in the excess of 35 dB is achieved due to the utilization of F2 devices for the driver transistors.

Drain Gate Feedback

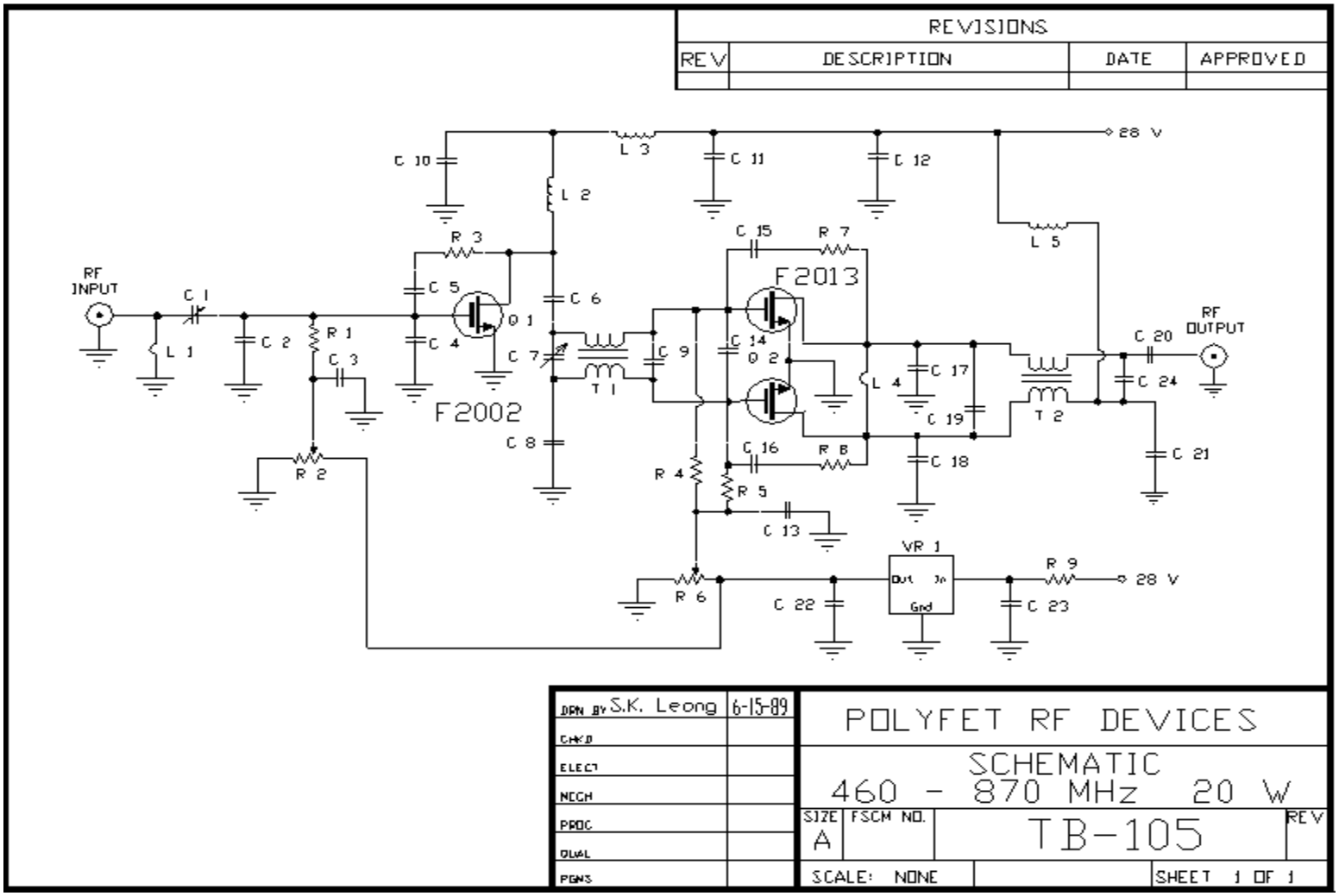
Drain gate feedback improves the stability of a MOSFET by using feedback to reduce the negative resistance of the active device by limiting the low frequency gain to a level which will not support oscillation with any input termination. This technique is very effective, but its use in circuitry intended for rapid rise times or high rates of AM modulation can cause severe envelope distortion. Also care must be used when choosing coupling capacitors. Too high a value can cause device failure during rapid circuit turn on. Noise figure is degraded when using this negative feedback. Examples of this technique can be found in TB 100 (R3/C3), TB 105 (R7/C15, R8/C16, R3/C5), etc.

TB 100



This is a one stage broad band amplifier using a F2001 transistor which utilizes negative feedback through R3 and R1 to achieve flat gain of 10 dB and approximately a 10 dB return loss from 1 - 1000 Mhz. The linear output power is one watt.

TB 105

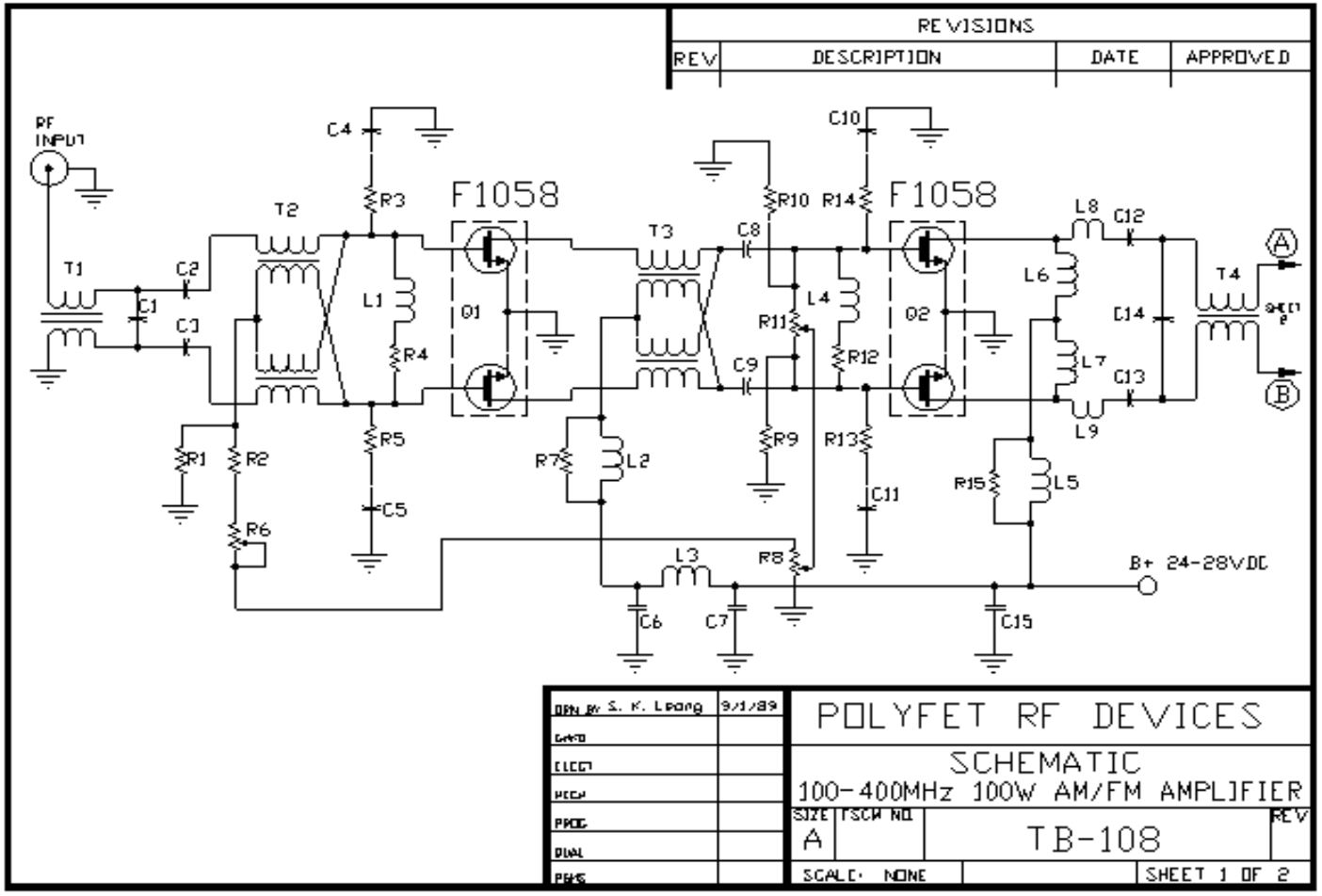


This is a two stage uhf television amplifier similar to TB 104 with an additional gain stage to cover the uhf television band with 18 dB gain.

Drain Shunt Resistance

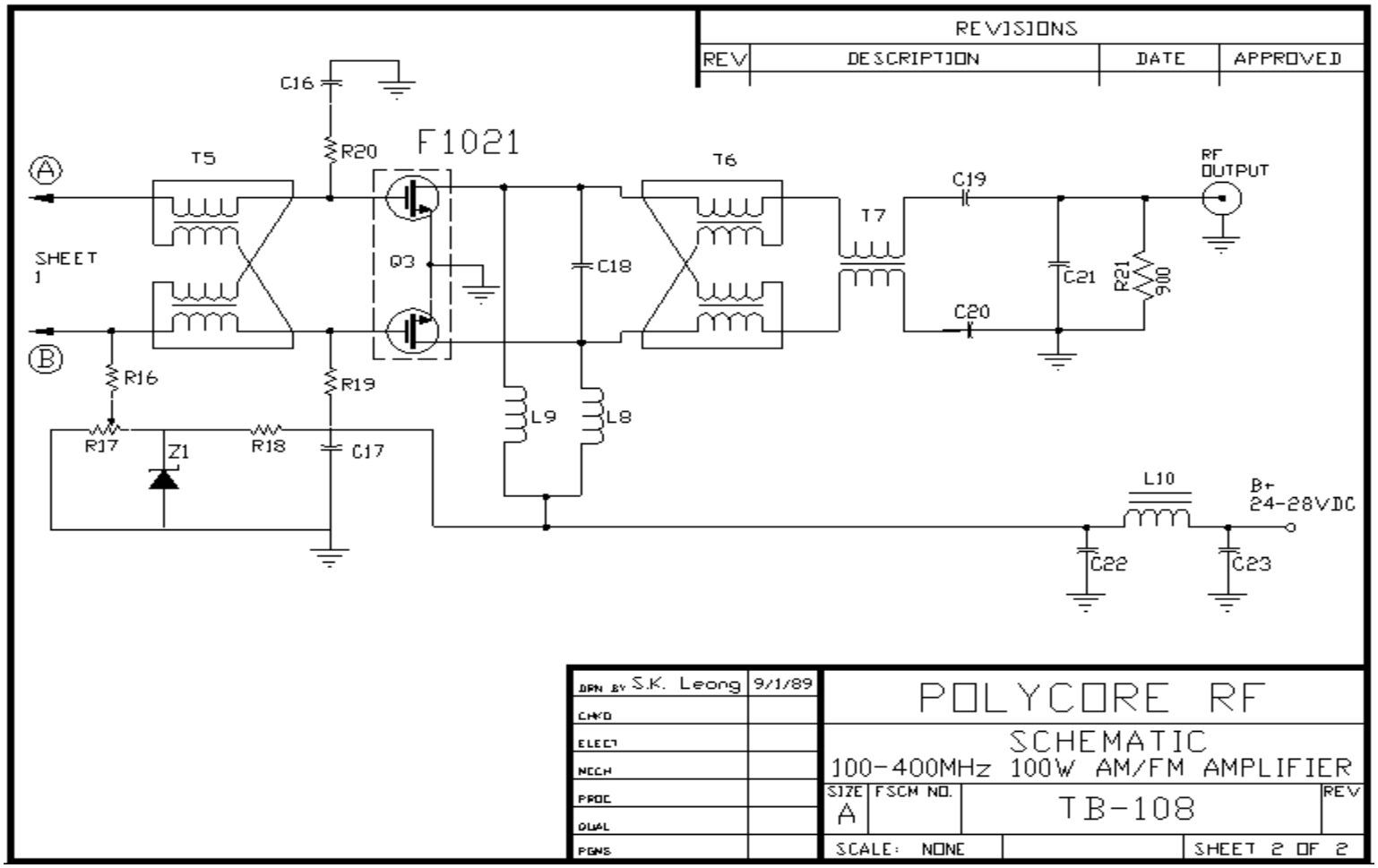
Drain shunt resistance terminates the drain in a low resistance which both lowers the effective gain of the device and reduces the Miller effect of the CRSS. Usually a shunt inductor is used to allow DC current to pass unobstructed and a series inductor to prevent loss of power at the operating frequency. This circuitry is useful if the power stage is subjected to moderate to high load VSWRs. Examples of this technique can be found in TB 107 (shunt-L4, series L2); TB 117 (L3 shunt, T3 series), TB 108A (shunt L5, series L6, L7) etc.

TB 108 A



This is a good example of a complete 100 - 400 MHz transmitter section of a 20 - 25 watt (80 - 100 watt) PEP transceiver capable of AM, FM or frequency hopping modulations with an input power of 100 milliwatts. It uses balanced devices throughout the design to minimize second harmonic generation which will simplify output filter design.

TB 108 B

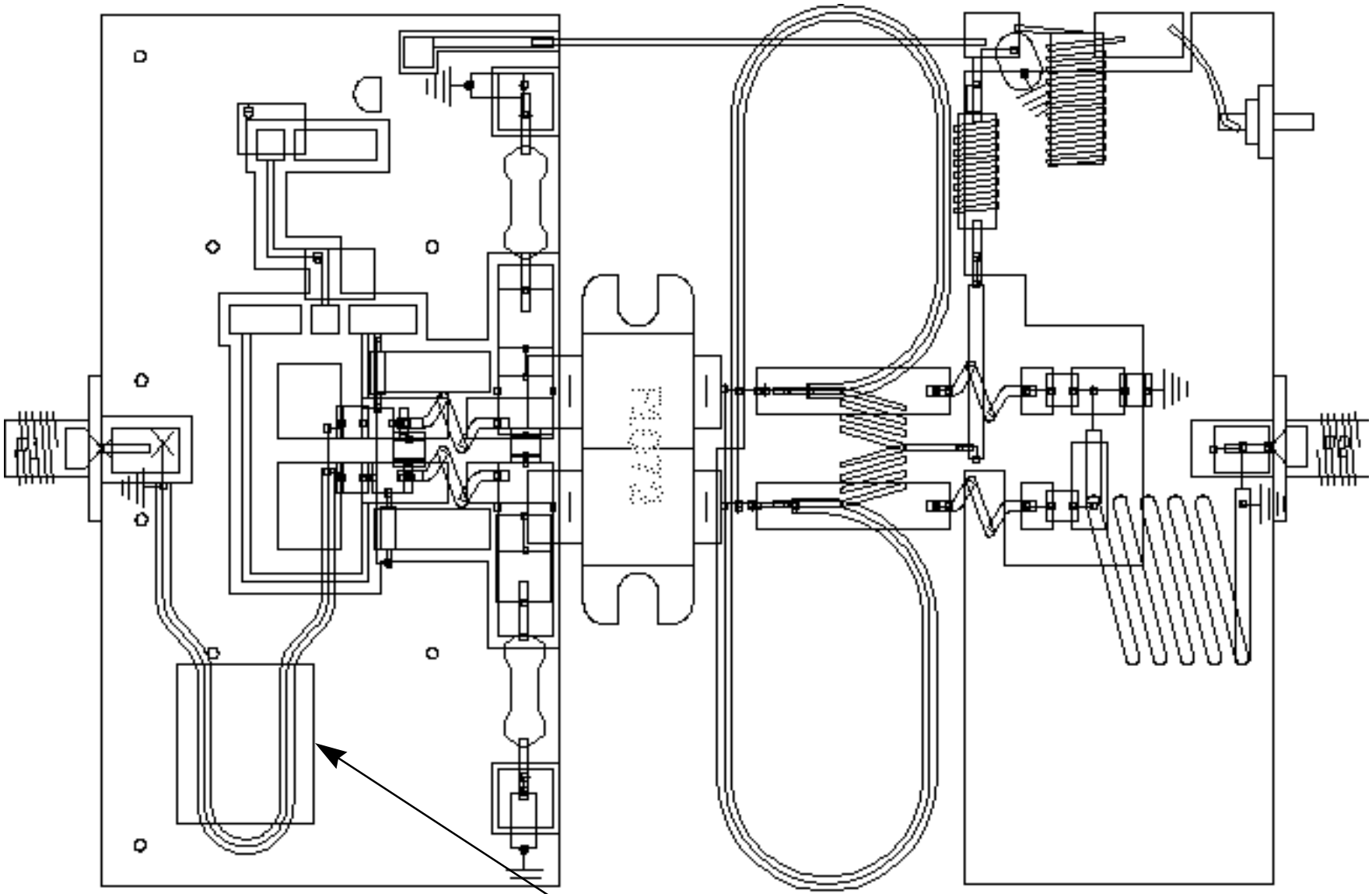


Continuation of TB-108 - a complete 100 - 400 MHz transmitter section of a 20 - 25 watt (80 - 100 watt)

Ferrite Loading (Gate Circuit)

Sometimes due to performance considerations, it may not be desirable to use series gate resistance. Shunt gate resistance is usually easy to implement, but gate resistance can cause a severe power gain loss. If the input circuit uses coaxial cables for impedance matching or power splitting, the coaxial cable can be ferrite loaded. This will have minimal effect at the operating frequency, but at lower frequencies, the ferrite will increase the series common mode input impedance. This will improve stability as a series gate resistance accomplishes. An example of this technique is TB 106.

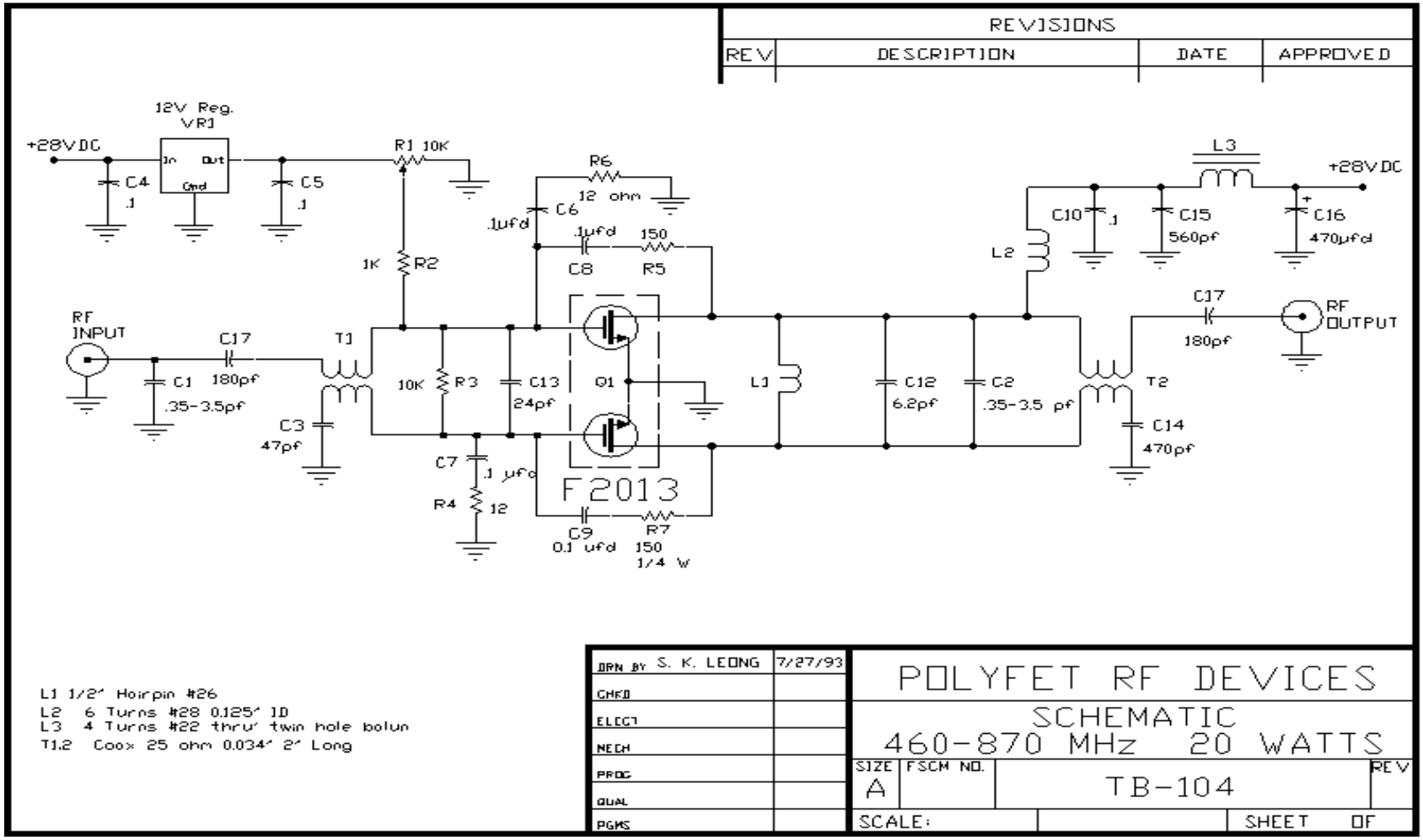
TB 106



Ferrite Loading (Drain Circuit)

Ferrite loading of the drain circuit is frequently used to improve stability under moderate to high VSWR load conditions. Ferrite loaded inductors are placed in the MOSFET drain's supply path to present a loss and a controlled impedance at frequencies below the operating band to control spurious generation during periods of high drain voltage during VSWR conditions. A standard circuit topology would be a series inductor off the drain to isolate the in band signals. Next is a ferrite loaded choke which is usually shunted by a resistor for additional damping. Examples of this technique can be found in TB 104 (series L2, choke L3).

TB 104



This is a balanced amplifier design intended for use in the television transposer or low power uhf television station designs. It utilizes distributed input and output matching networks for optimum bandwidth. It supplies 20 watt peak sync power with approximately 10 dB gain

Stability Analysis of input stabilization

F2012 VDMOS transistor

Freq	No stability circuit		Series Gate 1 ohm		Gate - Gnd 5 ohms		Series Gate 1 ohm Gate - Gnd 5 ohms		Drain - Gate 100 ohm		Series Gate 1 ohm Drain - Gate 100 ohm		Gate - Gnd 5 ohms Series Gate 1 ohm Drain - Gate 100 ohm	
Mhz	Stab	Gmax	Stab	Gmax	Stab	Gmax	Stab	Gmax	Stab	Gmax	Stab	Gmax	Stab	Gmax
100	0.156	25.653	0.231	25.653	7.405	13.967	4.249	16.42	1.106	17.115	1.14	16.822	2.519	12.254
200	0.287	22.716	0.445	22.716	3.539	14.306	2.291	16.329	1.088	17.179	1.165	16.526	2.377	12.42
300	0.453	21.031	0.693	21.031	2.18	14.884	1.734	16.048	1.076	17.205	1.215	16.083	2.189	12.717
400	0.585	19.886	0.916	19.886	1.388	16.176	1.474	15.809	1.029	17.588	1.252	15.621	1.904	13.171
500	0.793	19.14	1.229	16.253	1.102	17.199	1.558	14.744	1.041	17.155	1.359	14.81	1.77	13.297
600	0.93	18.348	1.457	14.34	0.983	18.348	1.672	13.559	1.036	16.763	1.444	13.964	1.703	13.031
700	1.112	15.884	1.749	12.893	1.188	15.298	2.014	12.17	1.087	15.791	1.589	13.085	1.852	12.265
800	1.319	13.917	2.058	11.438	1.689	12.459	2.525	10.449	1.19	14.324	1.769	11.87	2.197	10.776
900	1.353	13.191	2.15	10.662	2.12	10.732	2.843	9.334	1.21	13.665	1.839	11.139	2.48	9.663
1000	1.47	12.231	2.359	9.762	3.02	8.604	3.506	7.923	1.331	12.498	2.035	10.137	3.113	8.118
1100	1.46	11.508	2.359	8.999	3.686	6.933	3.876	6.708	1.388	11.428	2.103	9.173	3.55	6.717
1200	1.471	10.936	2.39	8.41	4.549	5.463	4.377	5.635	1.492	10.408	2.225	8.31	4.146	5.432
1300	1.599	9.959	2.585	7.54	6.023	3.725	5.339	4.257	1.667	9.069	2.438	7.156	5.022	3.865
1400	1.501	9.617	2.465	7.063	6.681	2.567	5.614	3.333	1.698	8.2	2.464	6.337	5.47	2.719
1500	1.361	9.572	2.292	6.772	7.325	1.524	5.844	2.516	1.72	7.457	2.481	5.631	5.976	1.656
1600	1.44	8.571	2.388	5.924	8.66	0.139	6.647	1.298	1.812	6.173	2.561	4.471	6.558	0.237
1700	1.354	8.212	2.235	5.498	8.998	-0.774	6.71	0.512	1.798	5.346	2.505	3.707	6.756	-0.761
1800	1.192	8.328	2.007	5.243	8.951	-1.537	6.512	-0.143	1.764	4.636	2.45	3.003	6.964	-1.704
1900	1.082	8.409	1.828	4.899	8.743	-2.252	6.258	-0.786	1.716	3.89	2.368	2.271	6.998	-2.62
2000	0.975	9.405	1.647	4.697	8.625	-2.949	6.05	-1.393	1.668	3.185	2.279	1.598	7.098	-3.54
2100	0.855	8.784	1.515	4.546	9.043	-3.777	6.19	-2.115	1.703	2.475	2.344	0.864	7.845	-4.577

Stability Analysis

1. No added circuitry. Unstable below 700 MHz
2. 1 ohm series gate resistor. Unstable below 400 Mhz
3. Shunt gate to gnd 5 ohms. Unstable at about 600 Mhz
4. 1 ohm series gate and 5 ohms shunt gate - gnd. All stable.
5. 100 ohm drain to gate feedback. All stable.
6. 1 ohm series gate plus 100 ohm drain to gate feedback. Stable - slightly lower gain.
7. All 3 resistors used. Stable - lower gain.