CD4066B CMOS Quad Bilateral Switch

1 Features

- 15-V Digital or ±7.5-V Peak-to-Peak Switching
- 125-Ω Typical On-State Resistance for 15-V Operation
- Switch On-State Resistance Matched to Within 5 Ω Over 15-V Signal-Input Range
- On-State Resistance Flat Over Full Peak-to-Peak Signal Range
- High ON/OFF Output-Voltage Ratio: 80 dB Typical at f_{is} = 10 kHz, R_L = 1 kΩ
- High Degree of Linearity: <0.5% Distortion Typical at f_{is} = 1 kHz, V_{is} = 5 V_{p-p} $V_{DD} - V_{SS} \geq 10$ V, R_L = 10 kΩ
- Extremely Low Off-State Switch Leakage, Resulting in Very Low Offset Current and High Effective Off-State Resistance: 10 pA Typical at $V_{DD} - V_{SS}$ = 10 V, T_A = 25°C
- Extremely High Control Input Impedance (Control Circuit Isolated From Signal Circuit): 10^{12} Ω Typical
- Low Crosstalk Between Switches: –50 dB Typical at f_{is} = 8 MHz, R_L = 1 kΩ
- Matched Control-Input to Signal-Output Capacitance: Reduces Output Signal Transients
- Frequency Response, Switch On = 40 MHz Typical
- 100% Tested for Quiescent Current at 20 V
- 5-V, 10-V, and 15-V Parametric Ratings

2 Applications

- Analog Signal Switching/Multiplexing: Signal Gating, Modulators, Squelch Controls, Demodulators, Choppers, Commutating Switches
- Digital Signal Switching/Multiplexing
- Transmission-Gate Logic Implementation
- Analog-to-Digital and Digital-to-Analog Conversions
- Digital Control of Frequency, Impedance, Phase, and Analog-Signal Gain

3 Description

The CD4066B device is a quad bilateral switch intended for the transmission or multiplexing of analog or digital signals. It is pin-for-pin compatible with the CD4016B device, but exhibits a much lower on-state resistance. In addition, the on-state resistance is relatively constant over the full signal-input range.

The CD4066B device consists of four bilateral switches, each with independent controls. Both the p and the n devices in a given switch are biased on or off simultaneously by the control signal. As shown in Figure 17, the well of the n-channel device on each switch is tied to either the input (when the switch is on) or to V_{SS} (when the switch is off). This configuration eliminates the variation of the switch-transistor threshold voltage with input signal and, thus, keeps the on-state resistance low over the full operating-signal range.

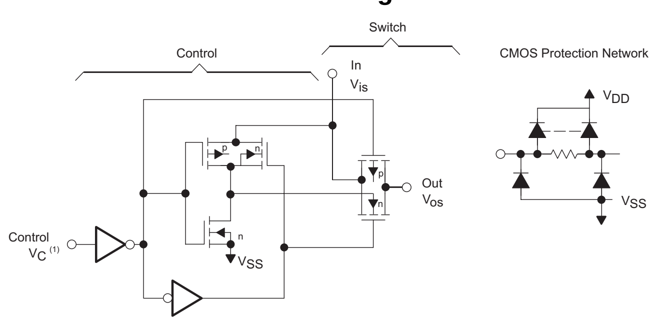
The advantages over single-channel switches include peak input-signal voltage swings equal to the full supply voltage and more constant on-state impedance over the input-signal range. However, for sample-and-hold applications, the CD4016B device is recommended.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
CD4066B	PDIP (14)	19.30 mm × 6.35 mm
	CDIP (14)	19.50 mm × 6.92 mm
	SOIC (14)	8.65 mm × 3.91 mm
	SOP (14)	10.30 mm × 5.30 mm
	TSSOP (14)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Bidirectional Signal Transmission Via Digital Control Logic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (September 2016) to Revision F — **Page**

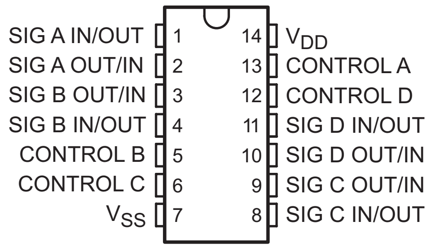
- Corrected the r_{on} V_{DD} = 10 V values in the *Electrical Characteristics* table. ... 7
- Corrected the y axis scale in Figure 6 ... 9

Changes from Revision D (September 2003) to Revision E — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Deleted *Ordering Information* table, see POA at the end of the data sheet ... 1
- Changed values in the *Thermal Information* table to align with JEDEC standards ... 4

5 Pin Configuration and Functions

N, J, D, NS, or PW Packages
14-Pin PDIP, CDIP, SOIC, SO, or TSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	SIG A IN/OUT	I/O	Input/Output for Switch A
2	SIG A OUT/IN	I/O	Output/Input for Switch A
3	SIG B OUT/IN	I/O	Output/Input for Switch B
4	SIG B IN/OUT	I/O	Input/Output for Switch B
5	CONTROL B	I	Control pin for Switch B
6	CONTROL C	I	Control pin for Switch C
7	V_{SS}	—	Low Voltage Power Pin
8	SIG C IN/OUT	I/O	Input/Output for Switch C
9	SIG C OUT/IN	I/O	Output/Input for Switch C
10	SIG D OUT/IN	I/O	Output/Input for Switch D
11	SIG D IN/OUT	I/O	Input/Output for Switch D
12	CONTROL D	I	Control Pin for D
13	CONTROL A	I	Control Pin for A
14	V_{DD}	—	Power Pin

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)]

			MIN	MAX	UNIT
V_{DD}	DC supply-voltage	Voltages referenced to V_{SS} pin	–0.5	20	V
V_{is}	Input voltage	All inputs	–0.5	V_{DD} + 0.5	V
I_{IN}	DC input current	Any one input		±10	mA
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[(1)]	±500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[(2)]	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{DD}	Supply voltage	3	18	V
T_A	Operating free-air temperature	–55	125	°C

6.4 Thermal Information

THERMAL METRIC[(1)]		CD4066B				UNIT
		N (PDIP)	D (SOIC)	NS (SO)	PW (TSSOP)	
		14 PINS	14 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	53.7	89.5	88.2	119.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	41.0	49.7	46.1	48.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	33.6	43.8	47.0	61.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	25.8	17.4	16.3	5.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	33.5	43.5	46.6	60.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{os}	Switch output voltage	V_{DD} = 5 V V_{is} = 0 V				0.4	V
		V_{DD} = 5 V V_{is} = 5 V		4.6			V
		V_{DD} = 10 V V_{is} = 0 V				0.5	V
		V_{DD} = 10 V V_{is} = 10 V		9.5			V
		V_{DD} = 15 V V_{is} = 0 V				1.5	V
		V_{DD} = 15 V V_{is} = 15 V		13.5			V
Δr_{on}	On-state resistance difference between any two switches	R_L = 10 kΩ, V_C = V_{DD}	V_{DD} = 5 V		15		Ω
			V_{DD} = 10 V		10		
			V_{DD} = 15 V		5		
THD	Total harmonic distortion	V_C = V_{DD} = 5 V, V_{SS} = –5 V, $V_{is(p-p)}$ = 5 V (sine wave centered on 0 V), R_L = 10 kΩ, f_{is} = 1-kHz sine wave			0.4%		
	–3-dB cutoff frequency (switch on)	V_C = V_{DD} = 5 V, V_{SS} = –5 V, $V_{is(p-p)}$ = 5 V (sine wave centered on 0 V), R_L = 1 kΩ			40		MHz
	–50-dB feedthrough frequency (switch off)	V_C = V_{SS} = –5 V, $V_{is(p-p)}$ = 5 V (sine wave centered on 0 V), R_L = 1 kΩ			1		MHz
	–50-dB crosstalk frequency	V_C(A) = V_{DD} = 5 V, V_C(B) = V_{SS} = –5 V, V_{is}(A) = 5 V_{p-p}, 50-Ω source, R_L = 1 kΩ			8		MHz
C_{is}	Input capacitance	V_{DD} = 5 V, V_C = V_{SS} = –5 V			8		pF
C_{os}	Output capacitance	V_{DD} = 5 V, V_C = V_{SS} = –5 V			8		pF
C_{ios}	Feedthrough	V_{DD} = 5 V, V_C = V_{SS} = –5 V			0.5		pF
V_{IHC}	Control input, high voltage	See Figure 7	V_{DD} = 5 V	3.5			V
			V_{DD} = 10 V	7			
			V_{DD} = 15 V	11			
	Crosstalk (control input to signal output)	V_C = 10 V (square wave), t_r, t_f = 20 ns, R_L = 10 kΩ V_{DD} = 10 V			50		mV
	Turnon and turnoff propagation delay	V_{IN} = V_{DD}, t_r, t_f = 20 ns, C_L = 50 pF, R_L = 1 kΩ	V_{DD} = 5 V		35	70	ns
			V_{DD} = 10 V		20	40	
			V_{DD} = 15 V		15	30	
	Maximum control input repetition rate	V_{is} = V_{DD}, V_{SS} = GND, R_L = 1 kΩ to GND, C_L = 50 pF, V_C = 10 V (square wave centered on 5 V), t_r, t_f = 20 ns, V_{os} = 1/2 V_{os} at 1 kHz	V_{DD} = 5 V		6		MHz
			V_{DD} = 10 V		9		
			V_{DD} = 15 V		9.5		
C_I	Input capacitance				5	7.5	pF

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{is}	Switch input current	V_{DD} = 5 V, V_{is} = 0 V	T_A = –55°C			0.64	mA
			T_A = –40°C			0.61	
			T_A = 25°C		0.51		
			T_A = 85°C			0.42	
			T_A = 125°C			0.36	
		V_{DD} = 5 V, V_{is} = 5 V	T_A = –55°C			–0.64	mA
			T_A = –40°C			–0.61	
			T_A = 25°C		–0.51		
			T_A = 85°C			–0.42	
			T_A = 125°C			–0.36	
		V_{DD} = 10 V, V_{is} = 0 V	T_A = –55°C			1.6	mA
			T_A = –40°C			1.5	
			T_A = 25°C		1.3		
			T_A = 85°C			1.1	
			T_A = 125°C			0.9	
		V_{DD} = 10 V, V_{is} = 10 V	T_A = –55°C			–1.6	mA
			T_A = –40°C			–1.5	
			T_A = 25°C		–1.3		
			T_A = 85°C			–1.1	
			T_A = 125°C			–0.9	
		V_{DD} = 15 V, V_{is} = 0 V	T_A = –55°C			4.2	mA
			T_A = –40°C			4	
			T_A = 25°C		3.4		
			T_A = 85°C			2.8	
			T_A = 125°C			2.4	
		V_{DD} = 15 V, V_{is} = 15 V	T_A = –55°C			–4.2	mA
			T_A = –40°C			–4	
			T_A = 25°C		–3.4		
			T_A = 85°C			–2.8	
			T_A = 125°C			–2.4	

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
I_{DD}	Quiescent device current	V_{IN} = 0 to 5 V, V_{DD} = 5 V		T_A = –55°C			0.25	µA
				T_A = –40°C			0.25	
				T_A = 25°C		0.01	0.25	
				T_A = 85°C			7.5	
				T_A = 125°C			7.5	
		V_{IN} = 0 to 10 V, V_{DD} = 10 V		T_A = –55°C			0.5	µA
				T_A = –40°C			0.5	
				T_A = 25°C		0.01	0.5	
				T_A = 85°C			15	
				T_A = 125°C			15	
		V_{IN} = 0 to 15 V, V_{DD} = 15 V		T_A = –55°C			1	µA
				T_A = –40°C			1	
				T_A = 25°C		0.01	1	
				T_A = 85°C			30	
				T_A = 125°C			30	
		V_{IN} = 0 to 20 V, V_{DD} = 20 V		T_A = –55°C			5	µA
				T_A = –40°C			5	
				T_A = 25°C		0.02	5	
				T_A = 85°C			150	
				T_A = 125°C			150	
r_{on}	On-state resistance (max)	$V_C = V_{DD}$, $R_L = 10\ k\Omega$ returned to $\frac{(V_{DD} - V_{SS})}{2}$, $V_{is} = V_{SS}$ to V_{DD}	V_{DD} = 5 V	T_A = –55°C			800	Ω
				T_A = –40°C			850	
				T_A = 25°C		470	1050	
				T_A = 85°C			1200	
				T_A = 125°C			1300	
			V_{DD} = 10 V	T_A = –55°C			310	
				T_A = –40°C			330	
				T_A = 25°C		180	400	
				T_A = 85°C			500	
				T_A = 125°C			500	
			V_{DD} = 15 V	T_A = –55°C			200	
				T_A = –40°C			210	
				T_A = 25°C		125	240	
				T_A = 85°C			300	
				T_A = 125°C			320	

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{ILC}	Control input, low voltage (max)	$\lvert I_{is}\rvert < 10\ \mu A$, $V_{is} = V_{SS}$, $V_{OS} = V_{DD}$, and $V_{is} = V_{DD}$, $V_{OS} = V_{SS}$	$V_{DD} = 5\ V$	$T_A = –55°C$		1		V
				$T_A = –40°C$		1		
				$T_A = 25°C$		1		
				$T_A = 85°C$		1		
				$T_A = 125°C$		1		
			$V_{DD} = 10\ V$	$T_A = –55°C$		2		
				$T_A = –40°C$		2		
				$T_A = 25°C$		2		
				$T_A = 85°C$		2		
				$T_A = 125°C$		2		
			$V_{DD} = 15\ V$	$T_A = –55°C$		2		
				$T_A = –40°C$		2		
				$T_A = 25°C$		2		
				$T_A = 85°C$		2		
				$T_A = 125°C$		2		
I_{IN}	Input current (max)	$V_{is} \le V_{DD}$, $V_{DD} – V_{SS} = 18\ V$, $V_{CC} \le V_{DD} – V_{SS}$ $V_{DD} = 18\ V$	$T_A = –55°C$				±0.1	µA
			$T_A = –40°C$				±0.1	
			$T_A = 25°C$			$\pm10^{-5}$	±0.1	
			$T_A = 85°C$				±1	
			$T_A = 125°C$				±1	

6.6 Switching Characteristics

$T_A = 25°C$

PARAMETER	FROM	TO	TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
t_{pd}	Signal input	Signal output	$V_{IN} = V_{DD}$, t_r, t_f = 20 ns, C_L = 50 pF, R_L = 1 kΩ	5 V		20	40	ns
				10 V		10	20	
				15 V		7	15	
t_{plh}	Signal input	Signal output	$V_{IN} = V_{DD}$, t_r, t_f = 20 ns, C_L = 50 pF, R_L = 1 kΩ	5 V		35	70	ns
				10 V		20	40	
				15 V		15	30	
t_{phl}	Signal input	Signal output	$V_{IN} = V_{DD}$, t_r, t_f = 20 ns, C_L = 50 pF, R_L = 1 kΩ	5 V		35	70	ns
				10 V		20	40	
				15 V		15	30	

6.7 Typical Characteristics

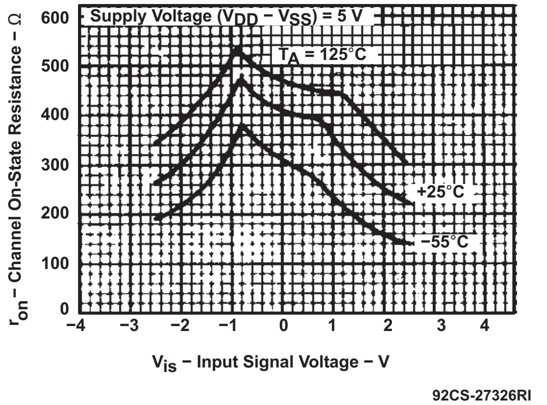


Figure 1. Typical ON-State Resistance vs Input Signal Voltage (All Types)

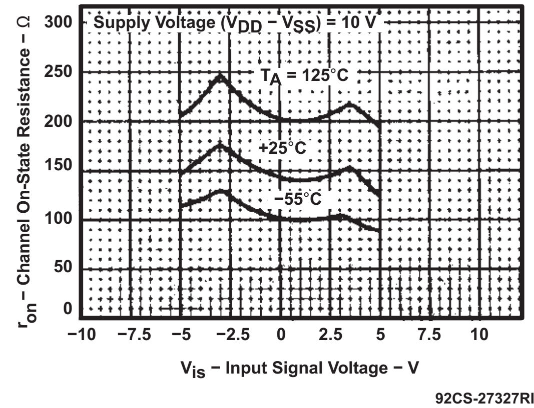


Figure 2. Typical ON-State Resistance vs Input Signal Voltage (All Types)

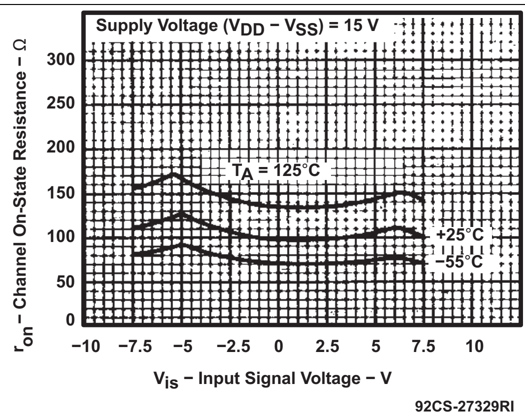


Figure 3. Typical ON-State Resistance vs Input Signal Voltage (All Types)

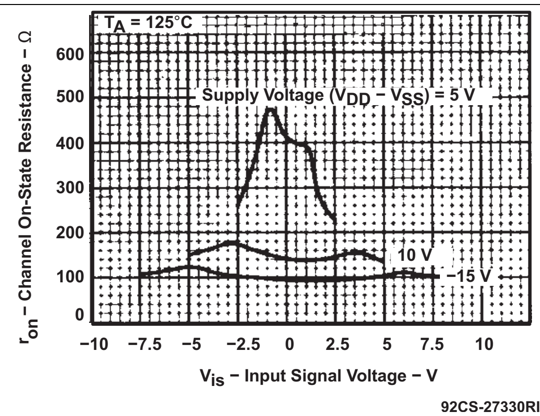


Figure 4. Typical ON-State Resistance vs Input Signal Voltage (All Types)

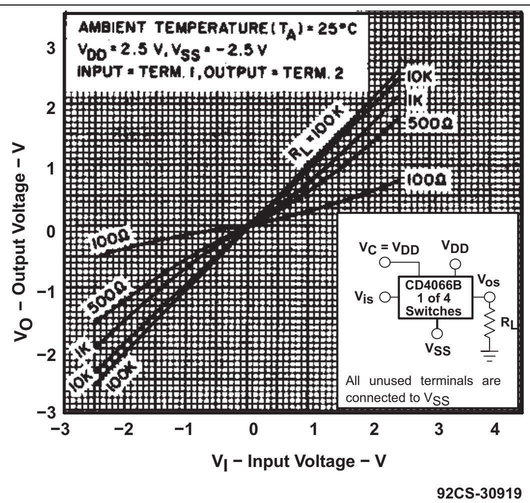


Figure 5. Typical ON Characteristics for 1 of 4 Channels

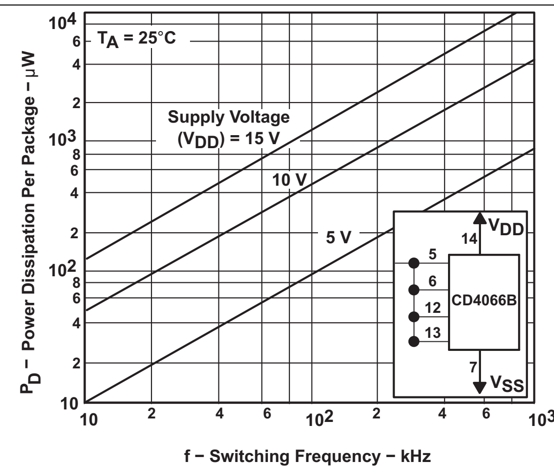


Figure 6. Power Dissipation per Package vs Switching Frequency

7 Parameter Measurement Information

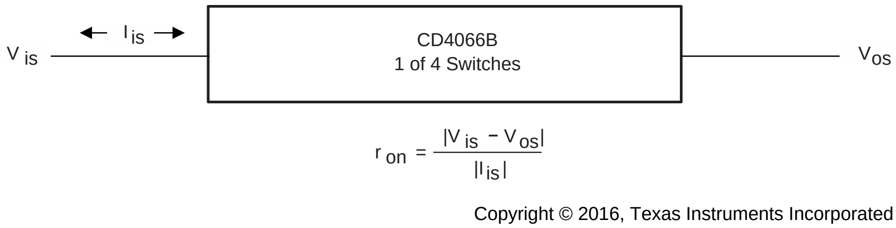


Figure 7. Determination of r_{on} as a Test Condition for Control-Input High-Voltage (V_{IHC}) Specification

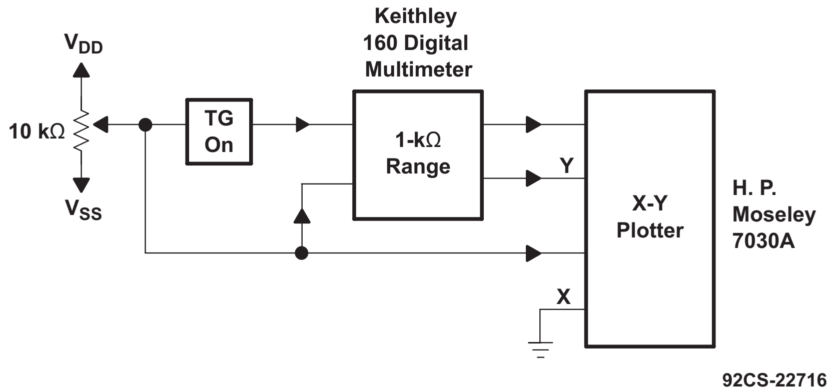
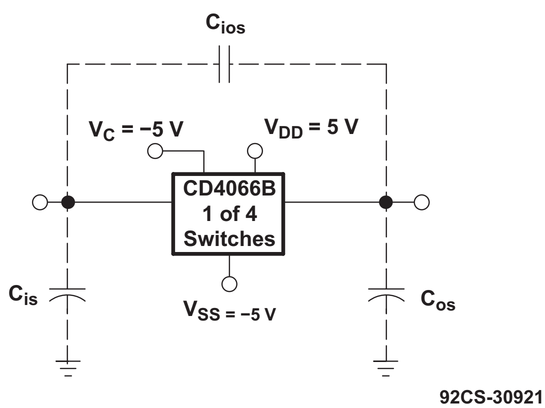


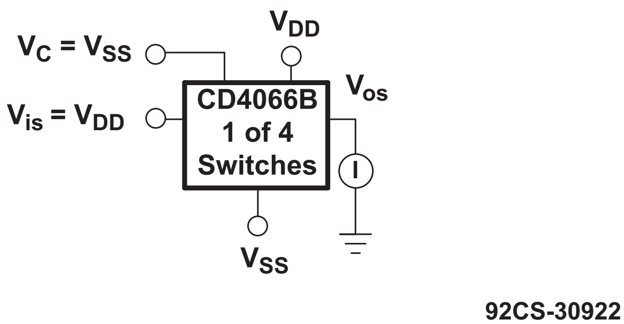
Figure 8. Channel On-State Resistance Measurement Circuit



Measured on Boonton capacitance bridge, model 75a (1 MHz);
test-fixture capacitance nulled out.

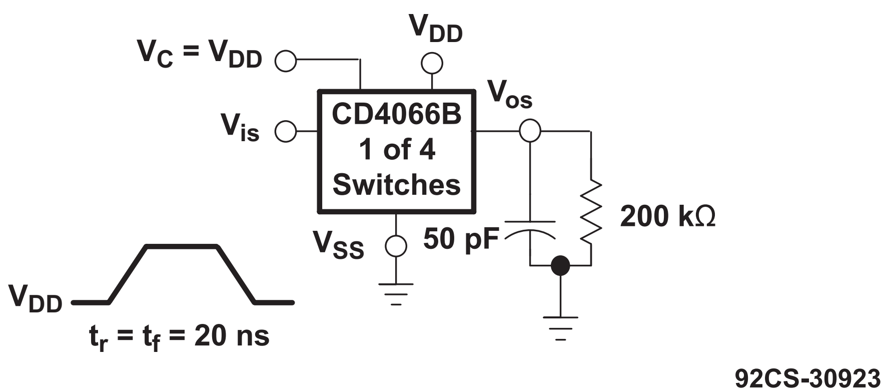
Figure 9. Typical On Characteristics for One of Four Channels

Parameter Measurement Information (continued)



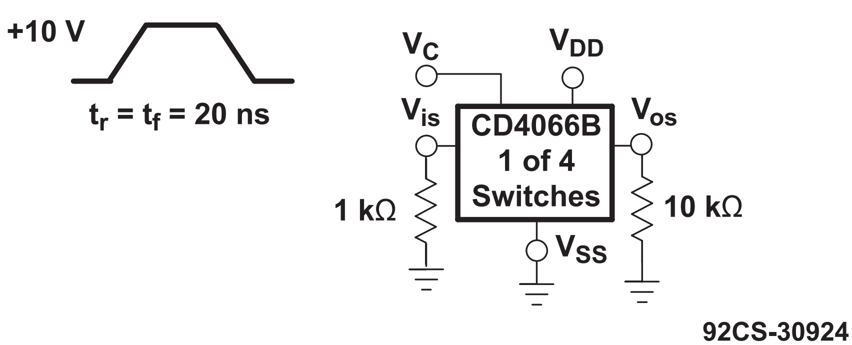
All unused terminals are connected to V_{SS}.

Figure 10. Off-Switch Input or Output Leakage



All unused terminals are connected to V_{SS}.

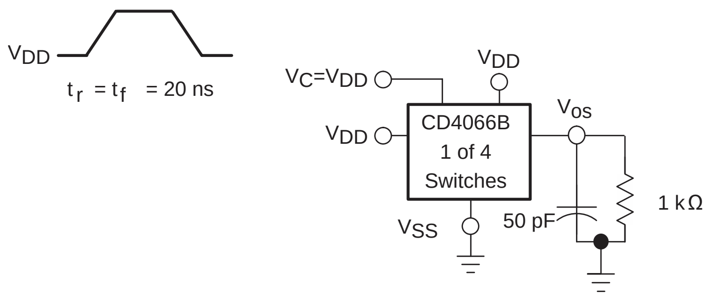
Figure 11. Propagation Delay Time Signal Input (V_{is}) to Signal Output (V_{os})



All unused terminals are connected to V_{SS}.

Figure 12. Crosstalk-Control Input to Signal Output

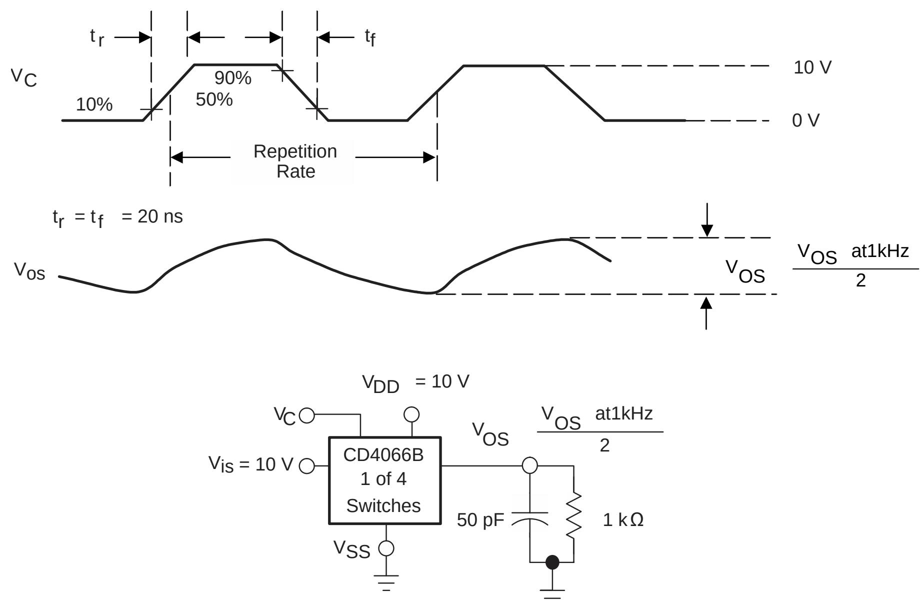
Parameter Measurement Information (continued)



All unused pins are connected to V_{SS}.

Delay is measured at V_{os} level of +10% from ground (turn-on) or on-state output level (turn-off).

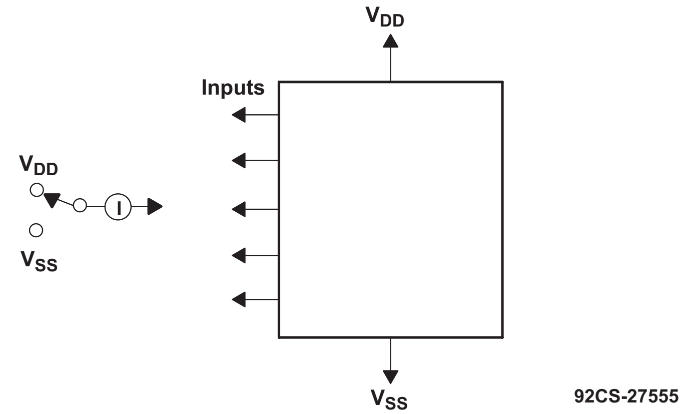
Figure 13. Propagation Delay, t_{PLH}, t_{PHL} Control-Signal Output



All unused pins are connected to V_{SS}.

Figure 14. Maximum Allowable Control-Input Repetition Rate

Parameter Measurement Information (continued)



Measure inputs sequentially to both V_{DD} and V_{SS}. Connect all unused inputs to either V_{DD} or V_{SS}. Measure control inputs only.

Figure 15. Input Leakage-Current Test Circuit

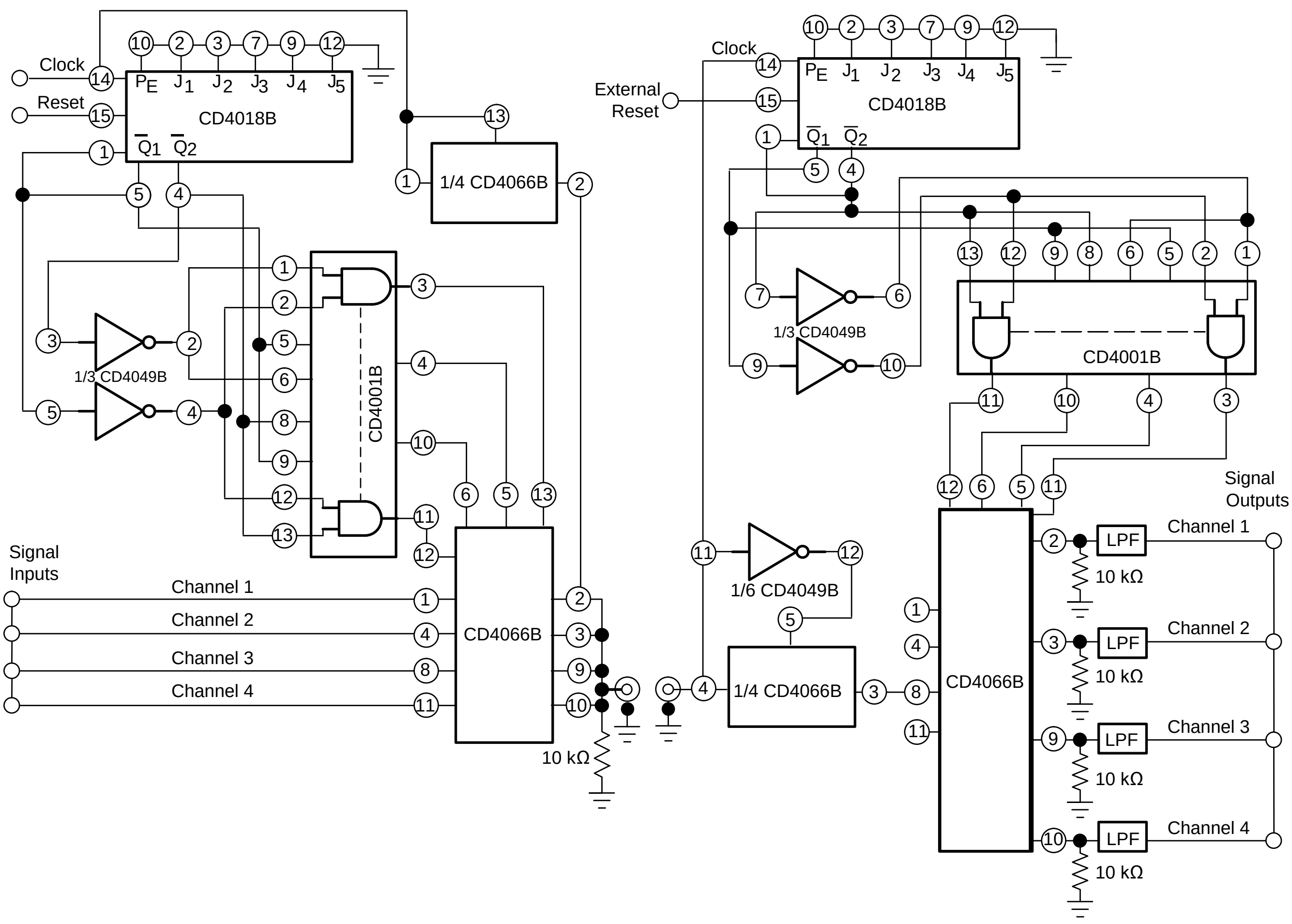


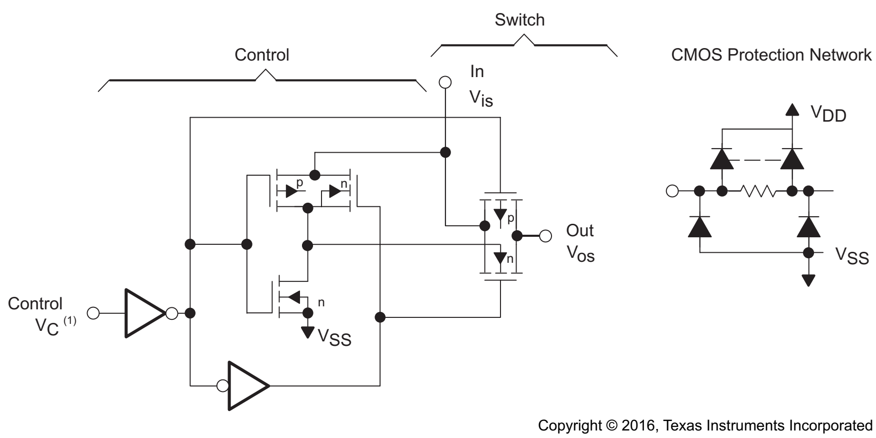
Figure 16. Four-Channel PAM Multiplex System Diagram

8 Detailed Description

8.1 Overview

CD4066B has four independent digitally controlled analog switches with a bias voltage of V_{SS} to allow for different voltage levels to be used for low output. Both the p and the n devices in a given switch are biased on or off simultaneously by the control signal. As shown in Figure 17, the well of the n-channel device on each switch is tied to either the input (when the switch is on) or to V_{SS} (when the switch is off). Thus when the control of the device is low, the output of the switch goes to V_{SS} while when the control is high the output of the device goes to V_{DD}.

8.2 Functional Block Diagram



(1) All control inputs are protected by the CMOS protection network.

(2) All p substrates are connected to V_{DD}.

(3) Normal operation control-line biasing: switch on (logic 1), $V_C = V_{DD}$; switch off (logic 0), $V_C = V_{SS}$.

(4) Signal-level range: $V_{SS} \le V_{is} \le V_{DD}$.

Figure 17. Schematic Diagram of One-of-Four Identical Switches and Associated Control Circuitry

8.3 Feature Description

Each switch has different control pins, which allows for more options for the outputs. Bias Voltage allows the device to output a voltage other than 0 V when the device control is low. The CD4066B has a large absolute maximum voltage for V_{DD} of 20 V.

8.4 Device Functional Modes

Table 1 lists the functions of this device.

Table 1. Function Table

INPUTS		OUTPUT
SIG IN/OUT	CONTROL	SIG OUT/IN
H	H	H
L	H	L
X	L	V_{SS}

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

In applications that employ separate power sources to drive V_{DD} and the signal inputs, the V_{DD} current capability should exceed V_{DD}/R_L (R_L = effective external load of the four CD4066B device bilateral switches). This provision avoids any permanent current flow or clamp action on the V_{DD} supply when power is applied or removed from the CD4066B device.

In certain applications, the external load-resistor current can include both V_{DD} and signal-line components. To avoid drawing V_{DD} current when switch current flows into pins 1, 4, 8, or 11, the voltage drop across the bidirectional switch must not exceed 0.8 V (calculated from r_{on} values shown).

No V_{DD} current flows through R_L if the switch current flows into pins 2, 3, 9, or 10.

9.2 Typical Application

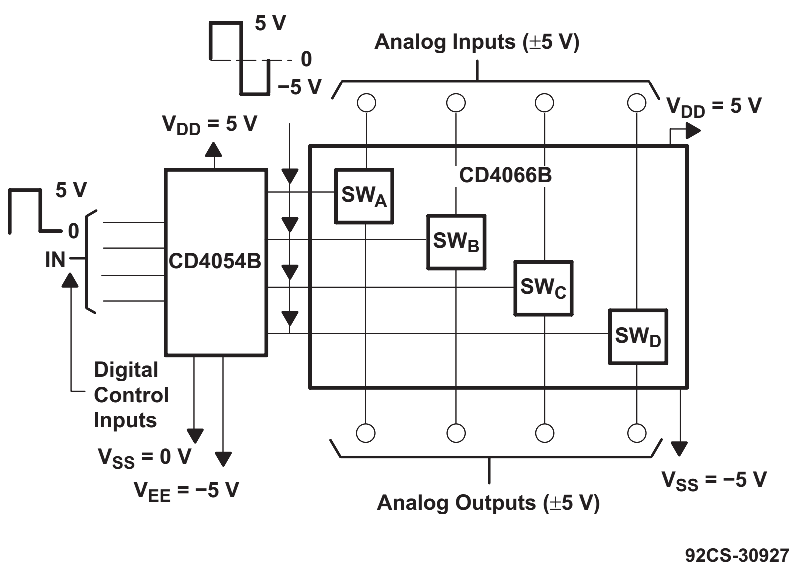


Figure 18. Bidirectional Signal Transmission Through Digital Control Logic

9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Avoid bus contention because it can drive currents in excess of maximum limits. The high drive also creates fast edges into light loads, so consider routing and load conditions to prevent ringing.

9.2.2 Detailed Design Procedure

1. Recommended Input Conditions:
   – For rise time and fall time specifications, see Δt/Δv in *Recommended Operating Conditions*.
   – For specified high and low levels, see V_{IH} and V_{IL} in *Recommended Operating Conditions*.
2. Recommended Output Conditions:
   – Load currents should not exceed ±10 mA.

Typical Application (continued)

9.2.3 Application Curve

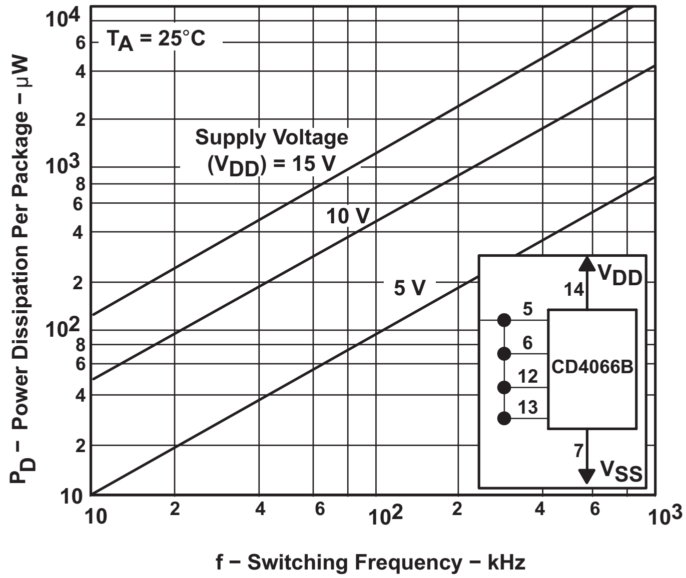


Figure 19. Power Dissipation vs. Switching Frequency

10 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in *Recommended Operating Conditions*.

Each VCC pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1-µF is recommended; if there are multiple VCC pins, then 0.01-µF or 0.022-µF is recommended for each power pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. A 0.1-µF and a 1-µF are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

11 Layout

11.1 Layout Guidelines

When using multiple bit logic devices inputs must never float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they are tied to GND or VCC, whichever makes more sense or is more convenient. It is generally acceptable to float outputs, unless the part is a transceiver. If the transceiver has an output enable pin, it disables the output section of the part when asserted. This does not disable the input section of the I/Os, so they cannot float when disabled.

11.2 Layout Example

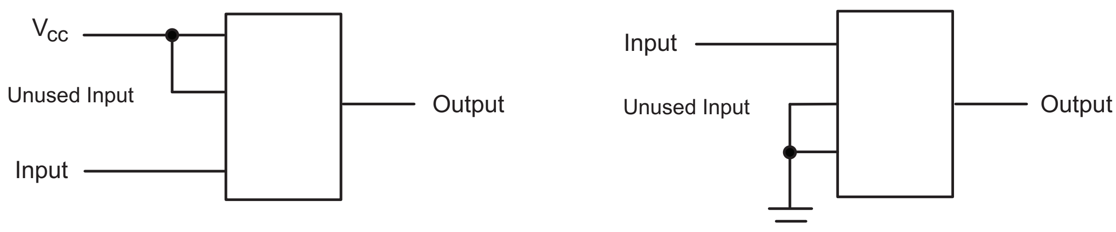


Figure 20. Diagram for Unused Inputs

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD4066BE	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU | CU SN	N / A for Pkg Type	-55 to 125	CD4066BE	Samples
CD4066BEE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD4066BE	Samples
CD4066BF	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	CD4066BF	Samples
CD4066BF3A	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	CD4066BF3A	Samples
CD4066BM	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4066BM	Samples
CD4066BM96	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-55 to 125	CD4066BM	Samples
CD4066BM96E4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4066BM	Samples
CD4066BM96G4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4066BM	Samples
CD4066BME4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4066BM	Samples
CD4066BMG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4066BM	Samples
CD4066BMT	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4066BM	Samples
CD4066BNSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4066B	Samples
CD4066BPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM066B	Samples
CD4066BPWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM066B	Samples
CD4066BPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-55 to 125	CM066B	Samples
CD4066BPWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM066B	Samples
JM38510/05852BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 05852BCA	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
M38510/05852BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 05852BCA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF CD4066B, CD4066B-MIL :

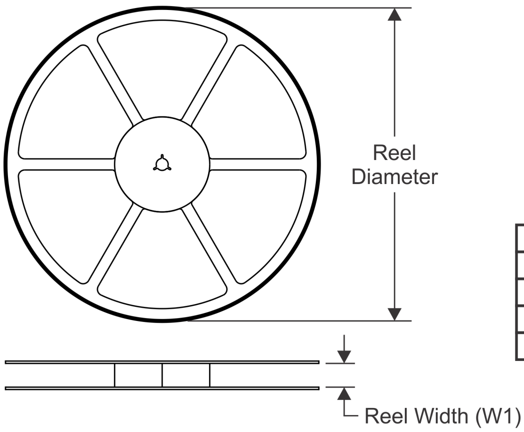
- Catalog: CD4066B
- Automotive: CD4066B-Q1, CD4066B-Q1
- Military: CD4066B-MIL

NOTE: Qualified Version Definitions:

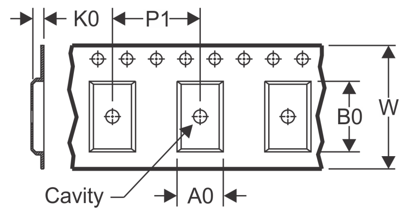
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

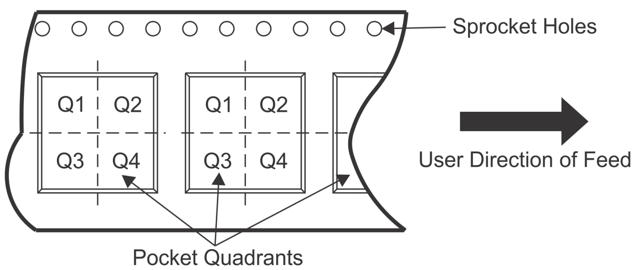


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

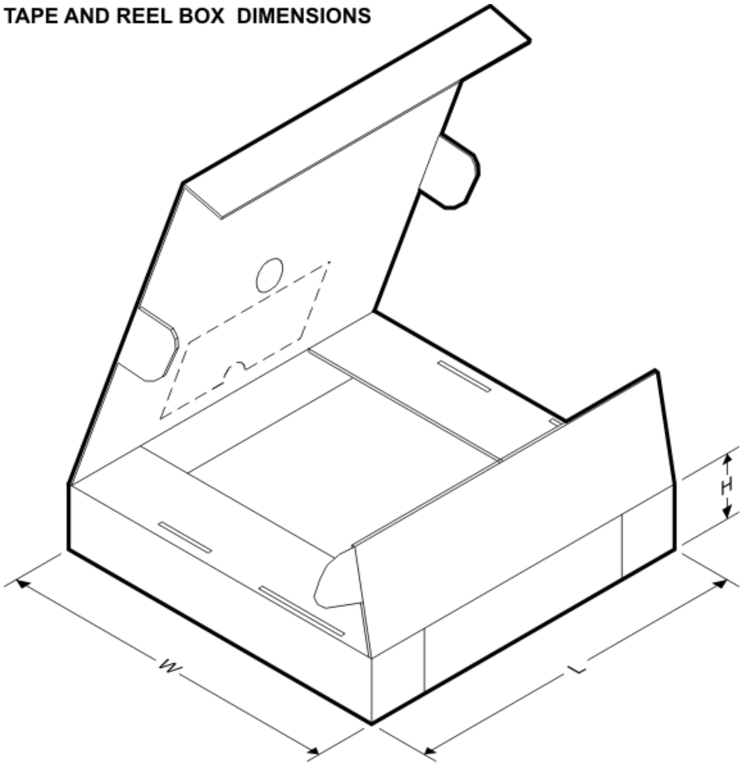
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4066BM96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD4066BM96	SOIC	D	14	2500	330.0	16.8	6.5	9.5	2.3	8.0	16.0	Q1
CD4066BM96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD4066BM96G4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD4066BM96G4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD4066BMT	SOIC	D	14	250	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD4066BNSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
CD4066BPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD4066BPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD4066BPWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

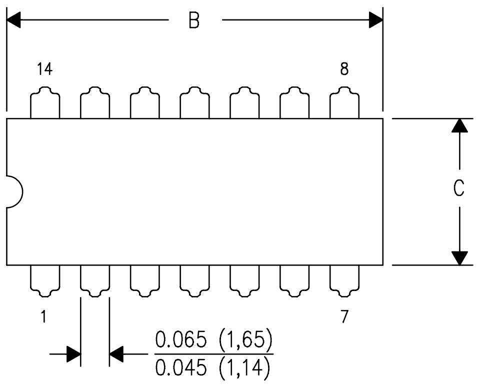


*All dimensions are nominal

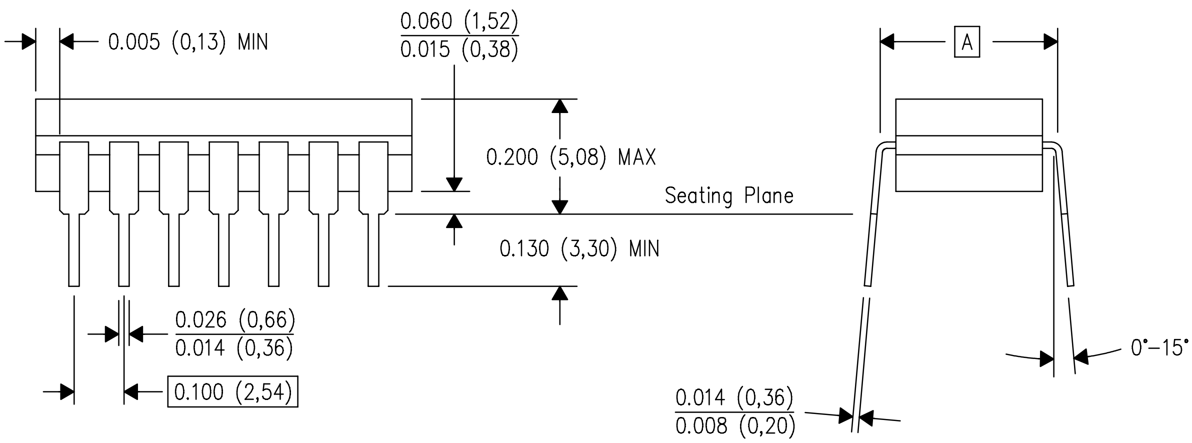
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4066BM96	SOIC	D	14	2500	333.2	345.9	28.6
CD4066BM96	SOIC	D	14	2500	364.0	364.0	27.0
CD4066BM96	SOIC	D	14	2500	367.0	367.0	38.0
CD4066BM96G4	SOIC	D	14	2500	333.2	345.9	28.6
CD4066BM96G4	SOIC	D	14	2500	367.0	367.0	38.0
CD4066BMT	SOIC	D	14	250	367.0	367.0	38.0
CD4066BNSR	SO	NS	14	2000	367.0	367.0	38.0
CD4066BPWR	TSSOP	PW	14	2000	364.0	364.0	27.0
CD4066BPWR	TSSOP	PW	14	2000	367.0	367.0	35.0
CD4066BPWRG4	TSSOP	PW	14	2000	367.0	367.0	35.0

J (R-GDIP-T**)   CERAMIC DUAL IN-LINE PACKAGE

14 LEADS SHOWN



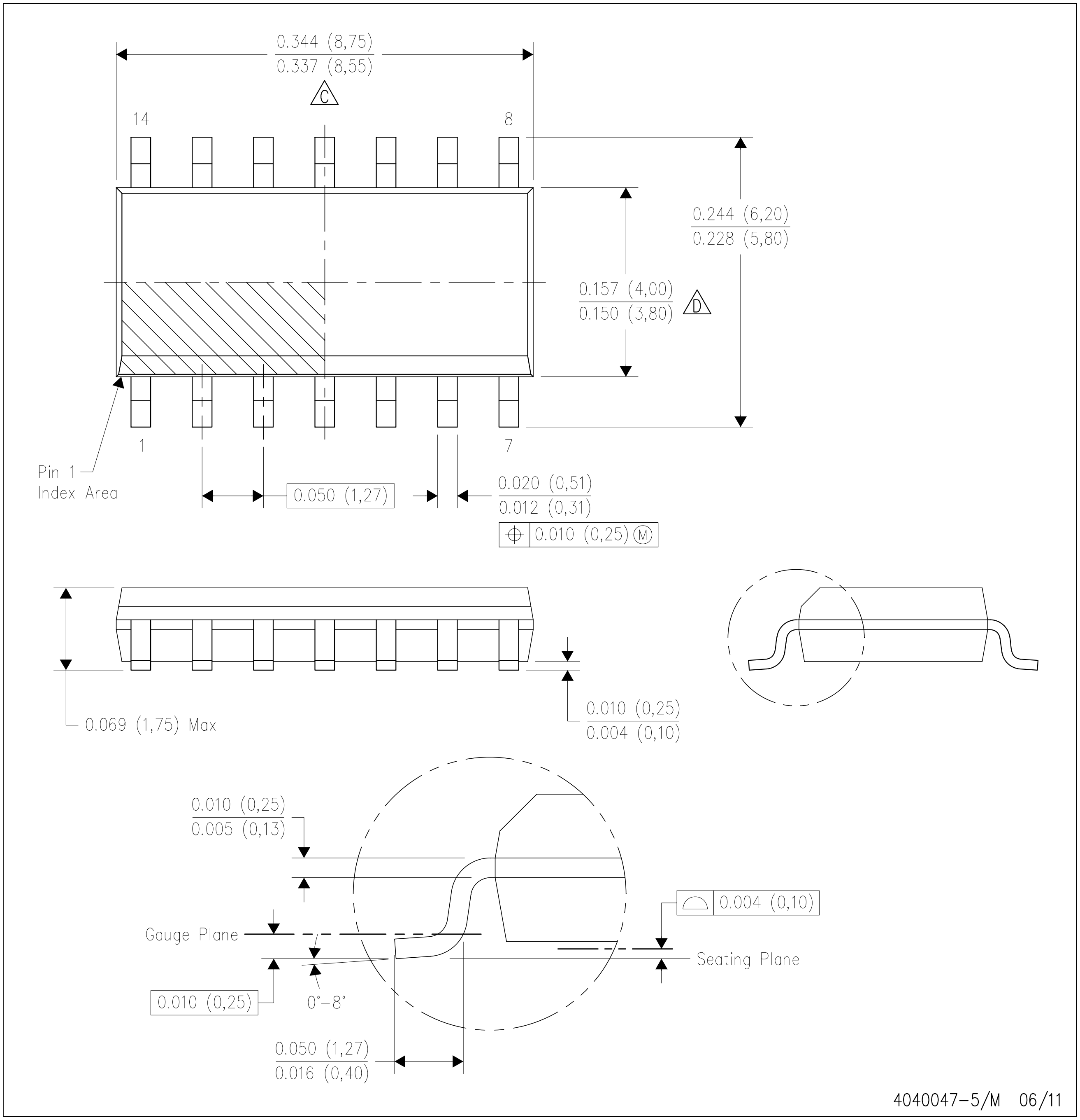
PINS ** / DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

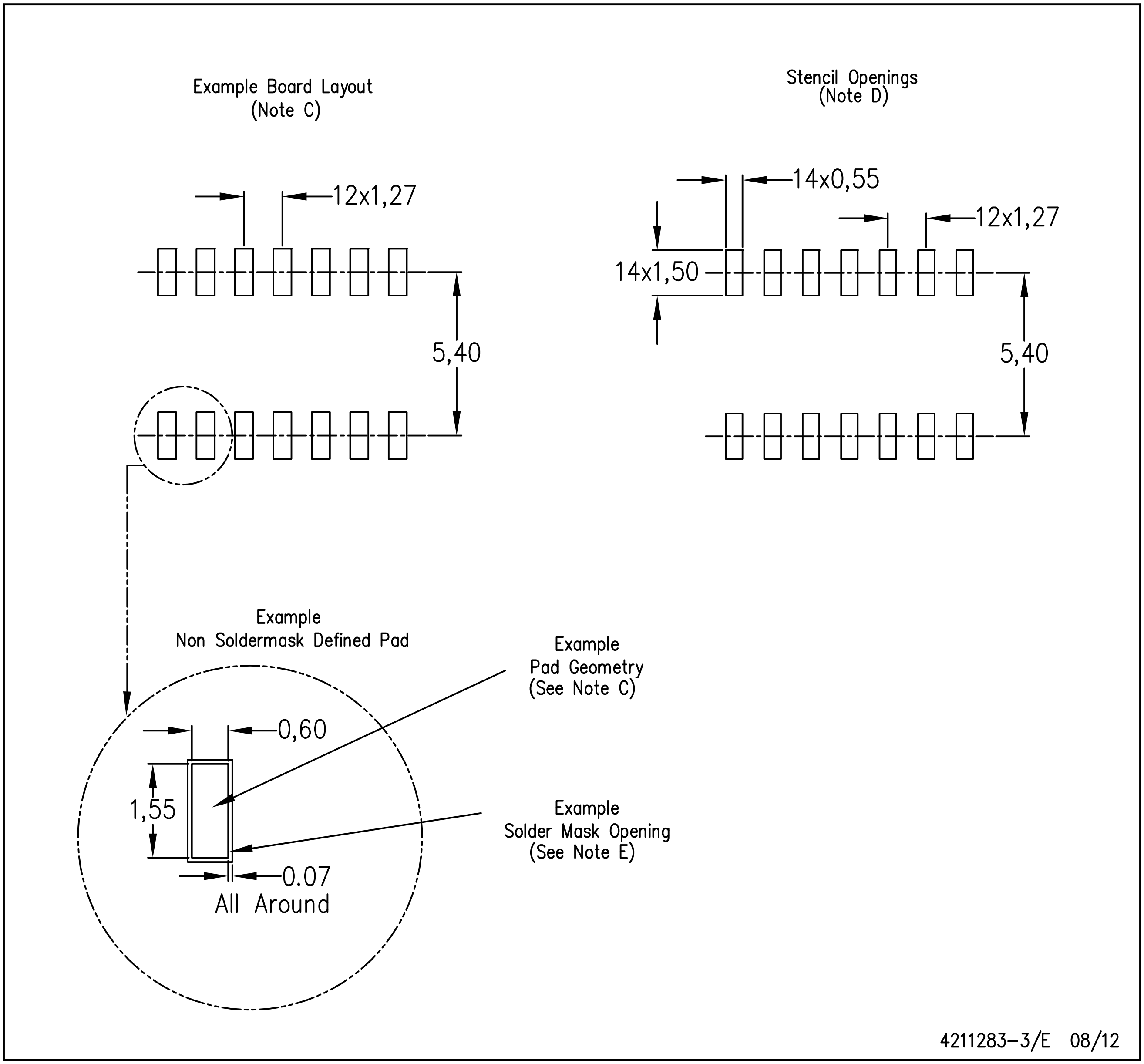
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



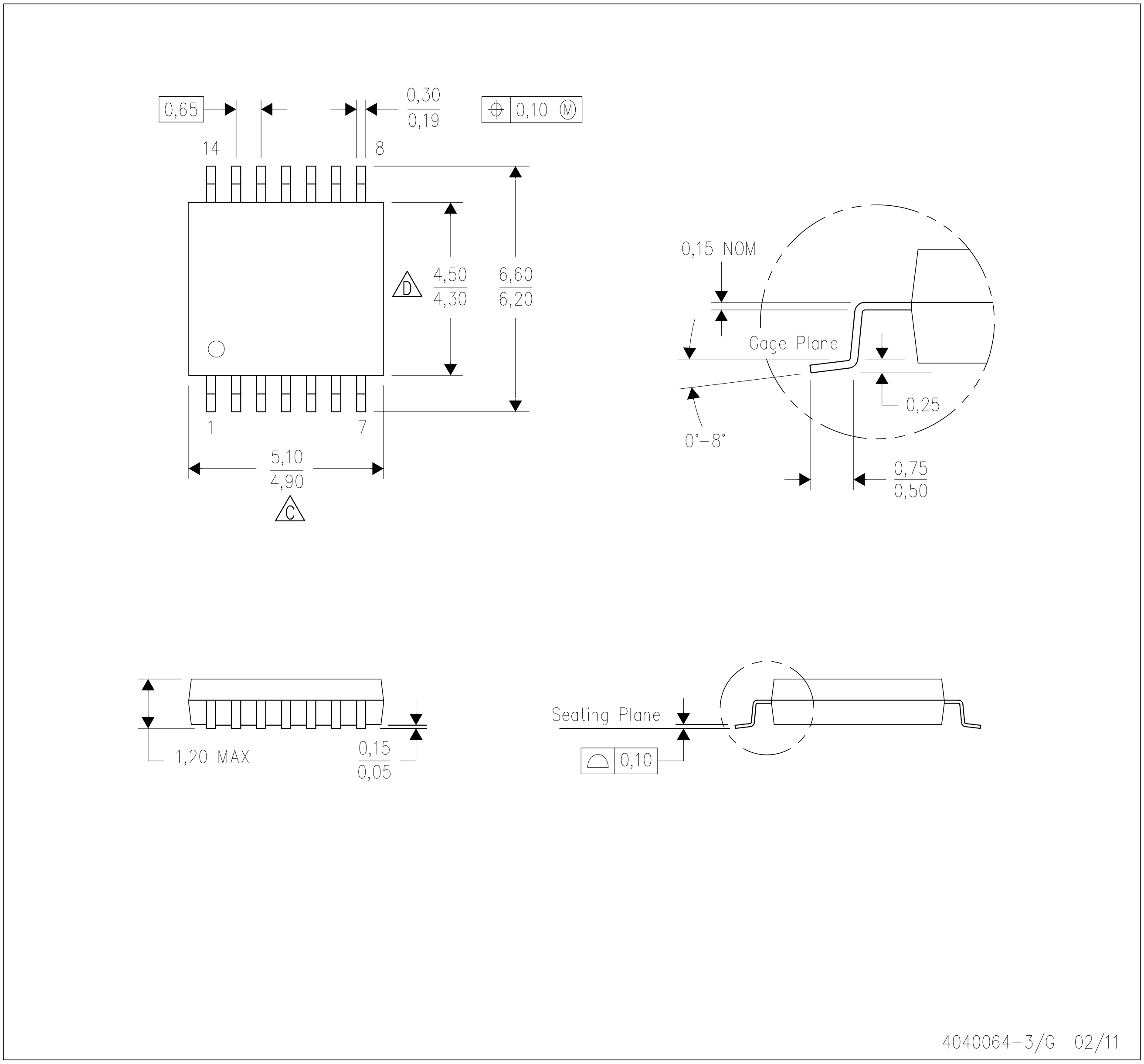
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



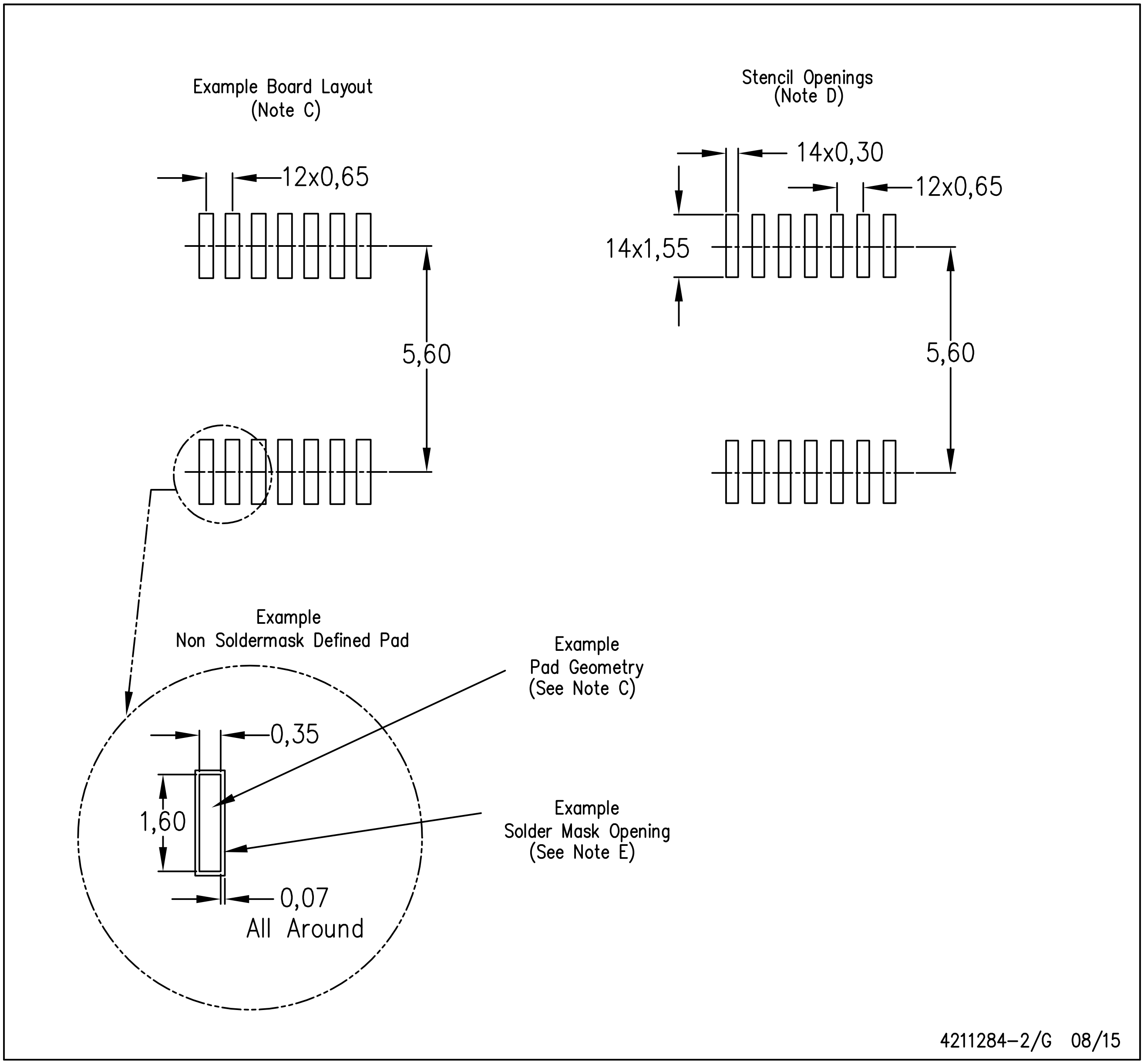
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R-PDSO-G14) PLASTIC SMALL OUTLINE

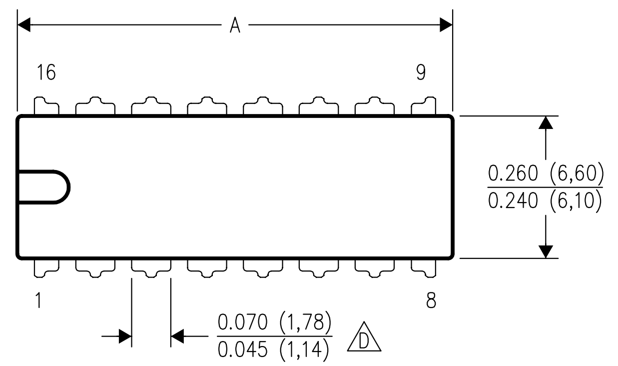


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

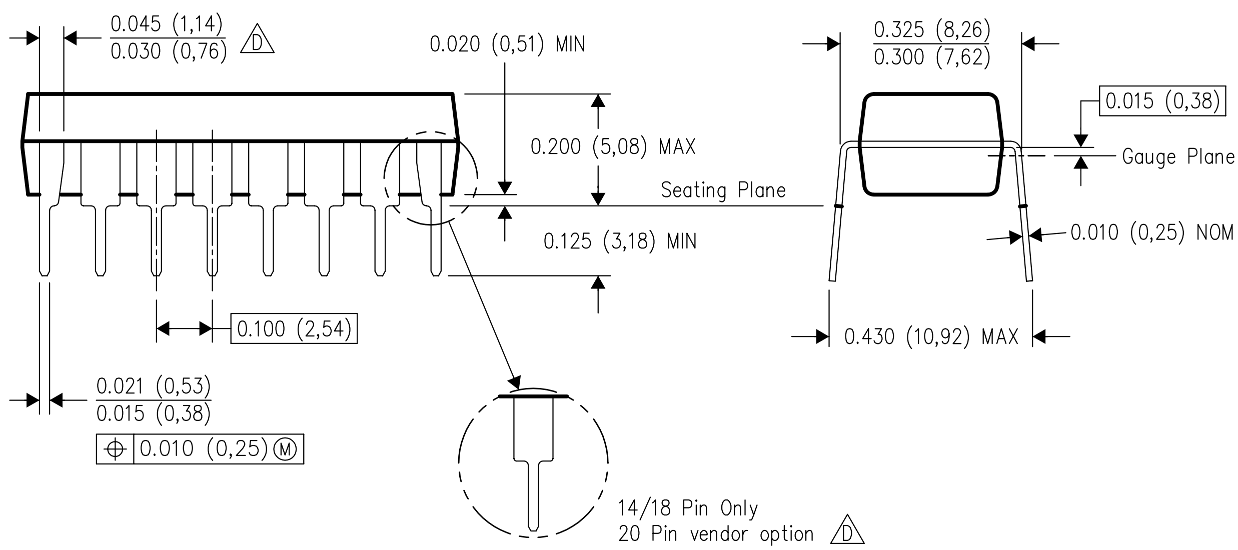
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



PINS ** / DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
C MS–001 VARIATION	AA	BB	AC	AD

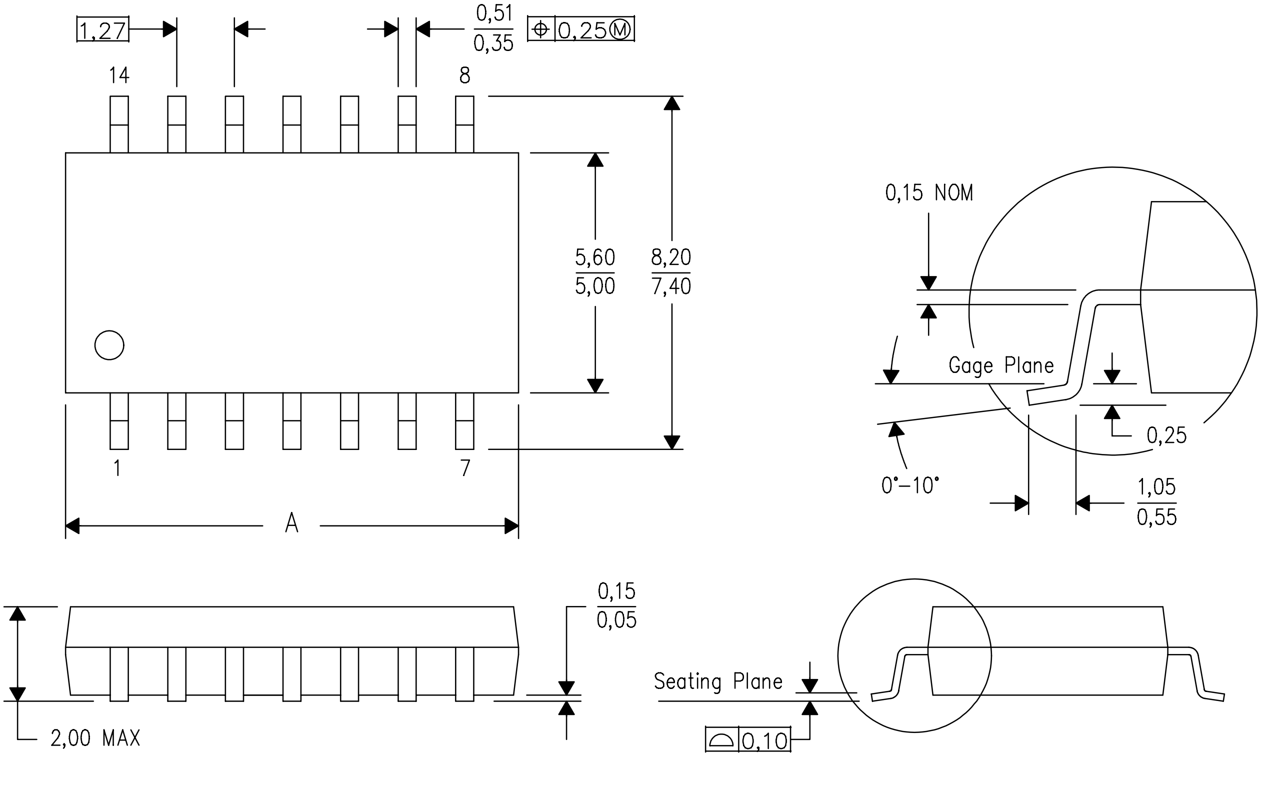


4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



PINS ** / DIM	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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